HTR Main FPGA
PCB: Rev4.3

Complete documentation on http://cmsdoc.cern.ch/cms/HCAL/document/CountingHouse/HTR/

Last changes in blu

FEATURES in NORMAL BEAM MODE

- One HTR board includes two identical logic sub-modules (Top and Bottom).
- Record a programmable **N**umber of QIE time-**S**amples (NS) and of **T**rigger **P**rimitives in response to a trigger.
- Zero-Suppression performed on ET, reduces the number of samples acquired. Individual threshold per channel
- L1A-trigger must arrive less than 6us after data (adjustable latency)
- TTC and VME access
- Reject triggers violating TDR rule 1 [No more than 1 trigger per 3 BXs] and 2 [No more than 2 triggers per 25 BXs]
- Overflow Warning (when buffer occupancy > 75%) and Busy flags.
- Empty Events generation (with correct EV#, BC# and ORBIT#) after Busy .
- Monitor fiber-to-fiber alignment with QIE_reset markers from the front-end.
- Support FE Orbit Message (Normal message only).
- TP Latency ~ 14 clock ticks (40 MHz clock) for the whole FPGA.
- Max average trigger rate (assuming no zero-sup.) ~ 1/ { [48xNS + 22] x 25 ns} ~ (1/NS) MHz

FEATURES in HISTOGRAMMING MODE

- used for detector calibration with radioactive source
- works only if the FrontEnd does not send orbit messages

FE / HTR Data format

From: http://www-ppd.fnal.gov/tshaw.myweb/CMS/FE/Prod/FE_v3.pdf

Last bit transmitted [GOL Ref. Manual - Version 1.6 , page 8].

Timing of D(24) is not 100% proven. Timing of IDLE-to-DATA is guaranteed.

In DATA mode bits D(16) and D(0) are constant, they are both received as LSB by the HTR, and they allow to distinguish the two 16-bit half-words received.
NB: that is not true in IDLE mode (or with Errors).

	D(31:30)	D(29:25)	D(24)	D(23:22)	D(21:17)	D(16)	D(15:14)	D(13:9)	D(8:7)	D(6:5)	D(4:3)	D(2)	D(1)	D(0)
Optical Cable 1	QIE 0 Exp (1:0)	QIE 0 Mant (4:0)	QIE_Reset (abort gap marker?)	QIE 1 Exp (1:0)	QIE 1 Mant (4:0)	"0"	QIE 2 Exp (1:0)	QIE 2 Mant (4:0)	QIE 0 CapID(1:0)	QIE 1 CapID(1:0)	QIE 2 CapID(1:0)	Control Flag=0	Data Flag=1	"1"
Optical Cable 2	QIE 4 Exp (1:0)	QIE 4 Mant (4:0)	QIE_Reset (abort gap marker?)	QIE 5 Exp (1:0)	QIE 5 Mant (4:0)	"0"	QIE 3 Exp (1:0)	QIE 3 Mant (4:0)	QIE 4 CapID(1:0)	QIE 5 CapID(1:0)	QIE 3 CapID(1:0)	Control Flag=0	Data Flag=1	"1"

FE DATA FORMAT

	D(31:25)	D(24)	D(23:21)	D(20)	D(19)	D(18:17)	D(16)	D(15:9)	D(8:7)	D(6:5)	D(4:3)	D(2)	D(1)	D(0)
Optical Cable 1	Bunch Count A (0:6)	QIE_Reset (abort gap marker?)	Bunch Count A (9:11)	Bunch Count Error A	CapID Error A	"XX"	"0"	Bunch Count B (0:6)	Bunch Count A (7:8)	"XX"	Bunch Count B (7:8)	Control Flag=1	Data Flag=0	"1"

	D(31:25)	D(24)	D(23:21)	D(20)	D(19)	D(18:17)	D(16)	D(15:13)	D(12)	D(11)	D(10:9)	D(8:7)	D(6:3)	D(2)	D(1)	D(0)
Optical Cable 2	Bunch Count C (0:6)	QIE_Reset (abort gap marker?)	Bunch Count C (9:11)	Bunch Count Error C	CapID Error C	"XX"	"0"	Bunch Count B (9:11)	Bunch Count Error B	CapID Error B	"XX"	Bunch Count C (7:8)	"XXXX"	Control Flag=1	Data Flag=0	"1"

FE Orbit Message - Normal message Supported

	D(31:25)	D(24)	D(23:17)	D(16)	D(15:9)	D(8)	D(7)	D(6:5)	D(4)	D(3)	D(2)	D(1)	D(0)
Optical Cable 1	Test Pattern "N" A(0:6)	QIE_Reset (abort gap marker?)	Test Pattern "N+1" A(1:7)	"0"	Test Pattern "N" B(0:6)	Test Pattern "N+1" A(0)	Test Pattern "N" A(7)	"XX"	Test Pattern "N+1" B(0)	Test Pattern "N" B(7)	Control Flag=0	Data Flag=1	"1"

	D(31:25)	D(24)	D(23:17)	D(16)	D(15:9)	D(8)	D(7)	D(6:2)	D(2)	D(1)	D(0)
Optical Cable 2	Test Pattern "N" C(0:6)	QIE_Reset (abort gap marker?)	Test Pattern "N+1" C(7:1)	"0"	Test Pattern "N+1" B(7:1)	Test Pattern "N+1" A(0)	Test Pattern "N" A(7)	"XXXX"	Control Flag=0	Data Flag=1	"1"

FE Orbit Message - Test Pattern message Not supported (treated as data)

HTR-DCC Data Format
May 2005 - from HTR v25 (normal mode)

Word Type	S1	S0	Byte 1	Byte 0
HEADER	1	1	SR | Zeroes	EvN [7:0]
Ext. Header2	1	0	EvN [23:16]	EvN [15:8]
Ext. Header3	1	0	1 | CT | HM | TM | | | | | BE	CK | OD | LW | LE | RL | EE | BZ | OW
Ext. Header4	1	0	OrN [5:0] | HTR_sub_module_Number[9:0]	
Ext. Header5	1	0	FormatVer[3:0] | BCN[11:8]	BCN [7:0]
Ext. Header6	1	0	Total # of TP words[7:0] after zero-sup.	NPS[4:0] # of PreSamples | DLLunlock[1:0] | TTCready
Ext. Header7	1	0	Firm. vers. #[18:16] | HTR Firmware version Number[12:0]	
Ext. Header8	1	0	Reserved (0…0)	PipeLength[7:0]
TP-DATA1	1	0	{FiberAd[2:0];ChAd[1:0]; Z; PS; TP[8:0]}	
…	1	0	…	
TP-DATAm	1	0	{FiberAd[2:0];ChAd[1:0]; Z; PS; TP[8:0]}	
DAQ-DATA1	1	0	{FiberAd[2:0]; QIE-Ad[1:0]; Er; DV; CapID[1:0]; QIE-range[1:0]; QIE-mantissa[4:0] }	
…			…	
DAQ-DATAn	1	0	{FiberAd[2:0]; QIE-Ad[1:0]; Er; DV; CapID[1:0]; QIE-range[1:0]; QIE-mantissa[4:0] }	
Parity word	1	0	Insert a word “FFFF” if zero-sup leads to an odd # of data words	
Extra-Info1	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber1 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber2 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber3 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber4 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber5 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber6 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber7 Orbit Message [11:0]
Extra-Info8	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber8 Orbit Message [11:0]
Pre-Trailer3	1	0	NS[4:0] =# of DaqData Samples (per L1A)	Total number of Daq words[10:0] after zero-sup.
Pre-Trailer2	1	0	Reserved	WordCount[11:0]
Pre-Trailer1	1	0	Zeroes	Zeroes
TRAILER	0	1	EvN [7:0]	Zeroes

See notes on next page

Notes about the HTR/DCC data format

Information relevant to DCC in the first and last 3 words. FormatVer[3:0] validated by Header3[15], compatible with existing data.
All relevant error bits should be concentrated on the word Ext. Header3. This word should contain future changes.
Ext. Header3 [8:0] is reported in the Common Data Format by the DCC.

SR = Status Request (from a TTC command, for the DCC LRB)
EvN = Counted internally. It should be = TTCrx EvN + 1
OW= Overflow Warning. Asserted when approching the Busy. If L1A rate is reduced the HTR should not go Busy.
BZ = Internal buffers are Busy, not necessarily related to the output data. Fast information, could be reported to the aTTS by the DCC.
EE = Empty Event (consequence of a past BZ). An **Empty Event** includes only the first 5 header words and the last 3 words.
RL = Rejected previous L1A (when previous L1A violates the trigger rules i and ii of Trigger TDR 16.4.3)
LE =Latency error (under development) ;
LW= Latency warning (under development);
OD = Optical Data error: this is a logic "OR" of all possible errors on the FE-Data (link, format, CapID). Reset after each HTR sub-fragment.
Note that depending on various settings this bit could be turned on by the orbit gap.
CK = An "OR" of various clocking problems (~TTCready, DLL_unlock, etc)
BE = Bunch Error: asserted if BCN is different from MaxBCN (that normally is 3563). Basically check if BCN wraps around correctly.
TM = Test Modes: can be CounterMode or PatternMode: if "0" real data; if "1" test data. L1As needed as in the real mode. Set from VME.
HM = Histogramming mode, need to change firmware to switch. It is a 0 in normal mode.
CT = Calibration Trigger event if 1 (L1A event if 0);
PS = Pattern Selected from RAMs (instead of real data)
Z = if "1", it means that the value of TP[8:0] sent to the SLB and RCT was zero (i.e. was not a peak).

DLL_unlock[2:0] = not functional. It should count of how many times the DLL unlocked since last Hard_rst.

FiberAd[2:0] indicates which fiber (0 to 7);
QIEAd[1:0] indicates which QIE channel in the fiber (0 to 2);
ChAd[1:0] is the Trigger Primitive channel address.

HTR-DCC Data Format
May 2005 - from HTR h6 (histogramming mode)

Word Type	S1	S0	Byte 1	Byte 0
HEADER	1	1	SR | Zeroes	EvN [7:0]
Ext. Header2	1	0	EvN [23:16]	EvN [15:8]
Ext. Header3	1	0	1 | CT | 1 | TM |	CK | OD | LW | LE | RL | EE | BZ | OW
Ext. Header4	1	0	OrN [5:0] | HTR_sub_module_Number[9:0]	
Ext. Header5	1	0	FormatVer[3:0] | BCN[11:8]	BCN [7:0]
Ext. Header6	1	0	0 | HistFib2[2:0] | 0 | HistFib1[2:0]	DLL_unlock[1:0] | TTCready
Ext. Header7	1	0	Firm. vers. #[18:16] | HTR Firmware version Number[12:0]	
Ext. Header8	1	0	Reserved (0…0)	FiberError[7:0]
TP-DATA1	1	0	{FiberAd[2:0];ChAd[1:0]; 0; PS; TP[8:0]}	
…	1	0	…	
TP-DATAm	1	0	{FiberAd[2:0];ChAd[1:0]; 0; PS; TP[8:0]}	
DAQ-DATA1	1	0	{FiberAd[2:0]; QIEAd[1:0]; Er; DV; CapID[1:0],QIEData[6:0] }	
…			…	
DAQ-DATAn	1	0	{FiberAd[2:0]; QIE Ad[1:0]; Er; DV; CapID[1:0],QIEData[6:0] }	
Parity word	1	0	Insert a word “FFFF” if zero-sup leads to an odd # of data words	
Extra-Info1	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber1 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber2 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber3 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber4 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber5 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber6 Orbit Message [11:0]
	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber7 Orbit Message [11:0]
Extra-Info8	1	0	{Empty, Full, LatCnt[1:0]}	Arrival time (BCN) of the Fiber8 Orbit Message [11:0]
	1	0	NS[4:0] =# of DaqData Samples (per L1A)	Total number of Daq words[10:0] after zero-sup.
	1	0	Reserved	WordCount[11:0]
Pre-Trailer	1	0	Zeroes	Zeroes
TRAILER	0	1	EvN [7:0]	Zeroes

FiberError[7:0] = 1 bit error summary per fiber. HistFib*[2:0] = which of the 8 input fibers is used for histogramming

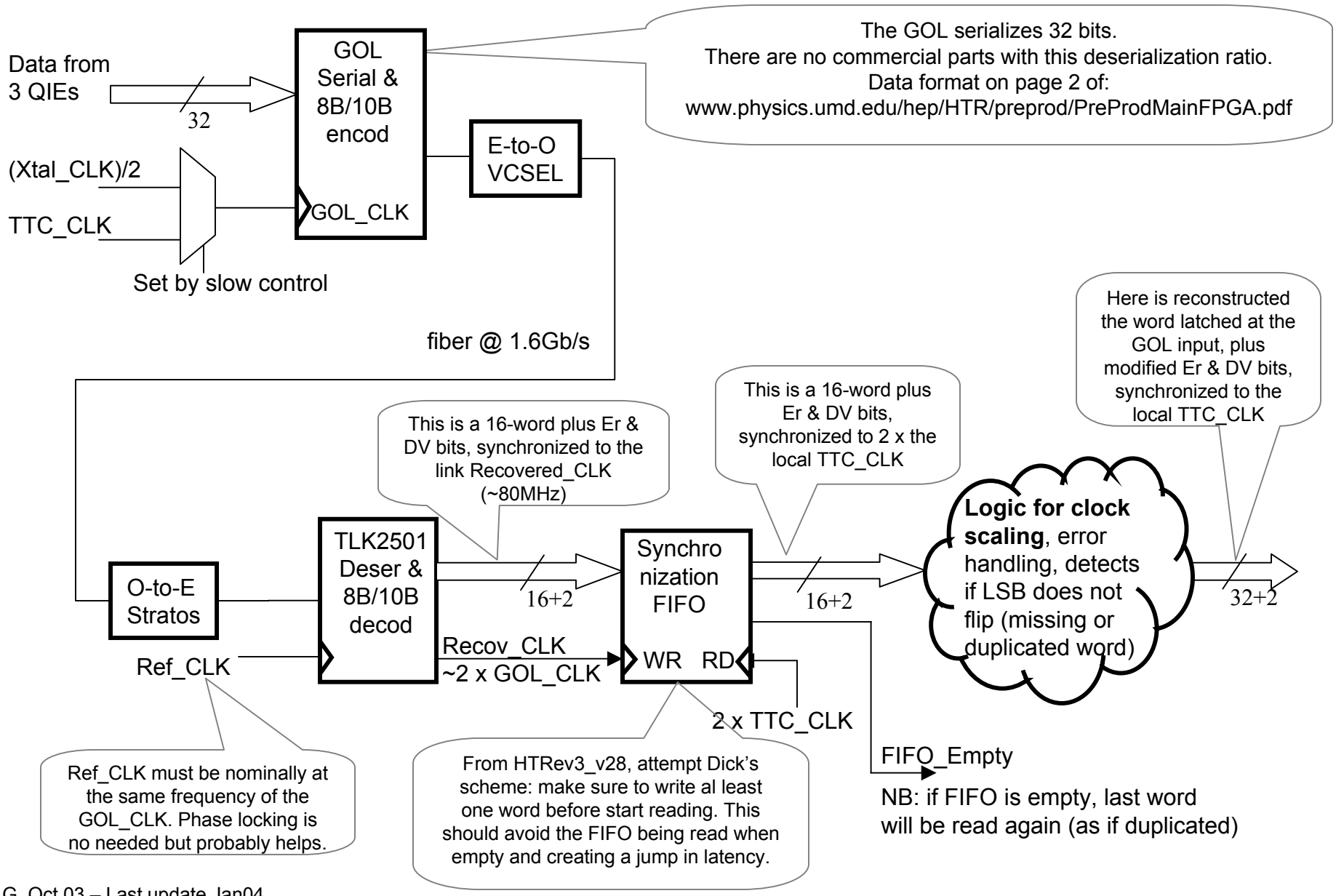
Quality of HTR data

Users of HTR data should verify that:

- bits Er = 0, DV = 1 in all DAQ-Data words
- TTCready = 1 in Ext. Header6
- the actual event size = WordCount[9:0] = (# of Daq-Data samples + # of TP samples) x 24 + 18
- For a given half-HTR, EvN [23:0] increases by 1 at every event
- EvN [23:0] is equal across all HTRs, if an EventCounterReset was issued by the TTC.
- DLL_unlock[2:0] does not increase from the previous event.

If this conditions are not verified, some debugging is needed. Please report the data to Tullio@umd.edu

FE-link logic diagram



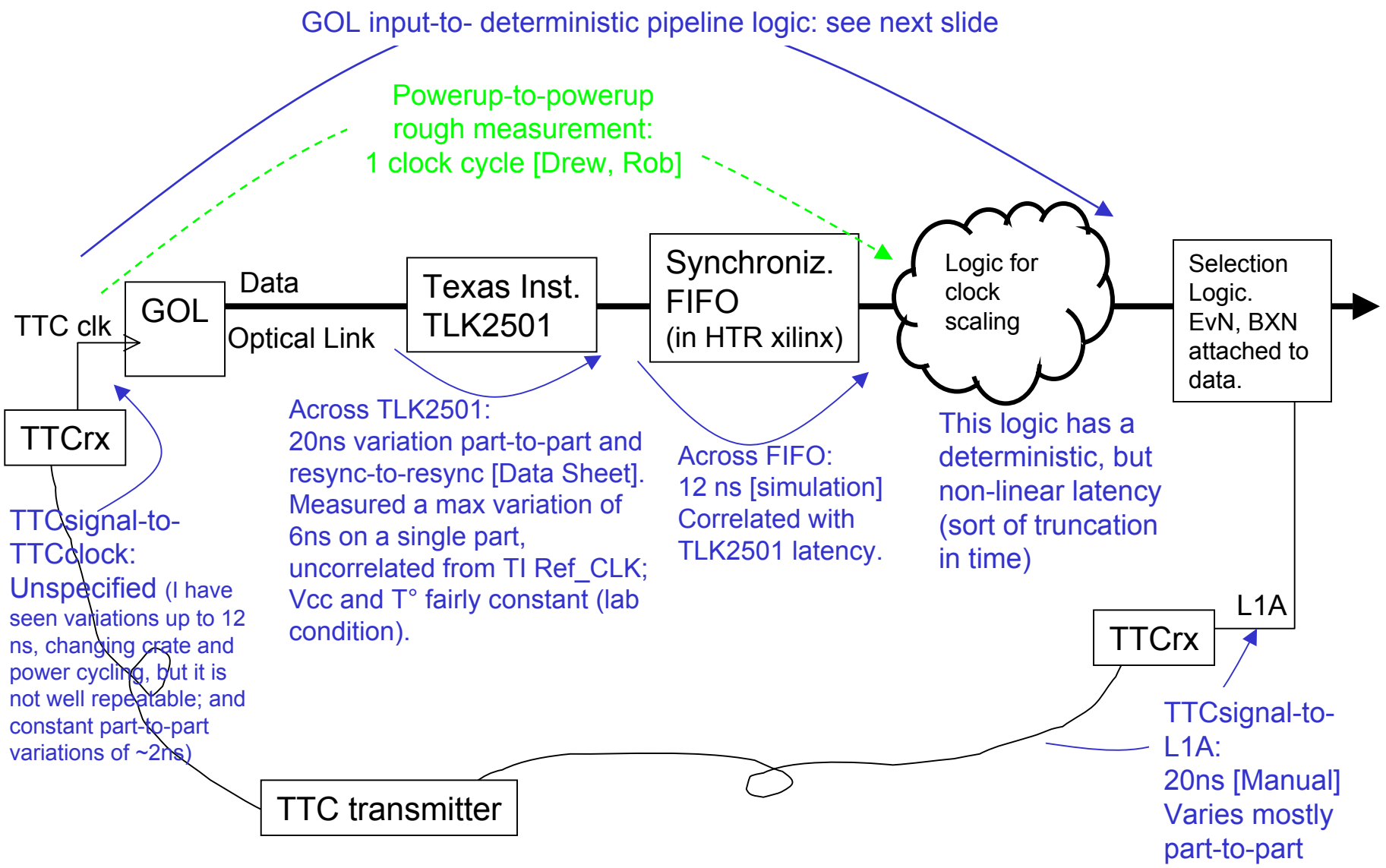
Optical Scheme

Date: Thu, 10 Jul 2003 11:05:50 -0500 (CDT)
From: Julie Whitmore <jaws@fnal.gov>
To: Tullio Grassi <tullio@Glue.umd.edu>
Cc: Drew Baden <drew@physics.umd.edu>, tshaw@fnal.gov Subject:
Re: fiber optic diagram

In the real system, the number of connections is somewhat larger than in the test beam. See my ESR presentation pages 21 & 22
http://www-ppd.fnal.gov/tshaw.myweb/CMS_Optical_Links.html (link to pdf file is at the bottom of the page)
[...]
In the real system, we have the following pieces (see ESR pp. 21&22):
1)Octopus inside RM (VCSEL to RM front panel)
2)Ribbon to patch panel [~20m] (fans-out at patch, but no fiber break)
3)Octopus inside patch panel (where channels are mapped)
4)Ribbon trunk to HTR [~70m]
5)Octopus on HTR
So the connections are
1)coupling to VCSEL, 2)coupling at RM front panel, 3)coupling at front of patch panel, 4)coupling at back of patch panel, 5)coupling at HTR front panel, 6) coupling to receiver.
The largest number of connections is with the calibration modules, where for some fibers we will have additional connections near the HTRs to try to fully populate the ribbon fibers. This is also true for the overlap regions of HB/HE, where we will have an additional patch panel to complete the mapping. I believe that adds an 2 extra connections (for the front and back part of the extra patch panel). So in the worst regions, we can have up to 8 connections. As for attenuation, the typical attenuation is 0.5dB per connection. The fiber attenuation is 2.5dB/km or 0.25dB for 100m. So we an exptect up to 3.25-4.25dB for the real system. Terri made a measurement with 10 connections and 150m of fiber. She measured 7.3dB attenuation, but she also had a 62.5um connection to her optical probe (fibers are 50um), where she said she expected to lose an additional ~3dB from her setup. So we expected 5.4dB and measured ~4.3dB (7.3dB - 3dB (for probe)).
I hope this information helps. –julie
==========
Date: Fri, 19 Dec 2003 16:37:40 -0600 (CST)
From: Julie Whitmore <jaws@fnal.gov>
To: Tullio Grassi <tullio@Glue.umd.edu>
Cc: Drew Baden <drew@physics.umd.edu>, Theresa Shaw <tshaw@fnal.gov>
Subject: Re: summary of tests
[CUT] I spec'd 50/125 graded-index multimode, which means that there is not an index of refraction interface at the core boundary (variable index of refraction out to 125um).[CUT] The fiber is Germanium doped Silicon.

Random Latency in HCAL electronics

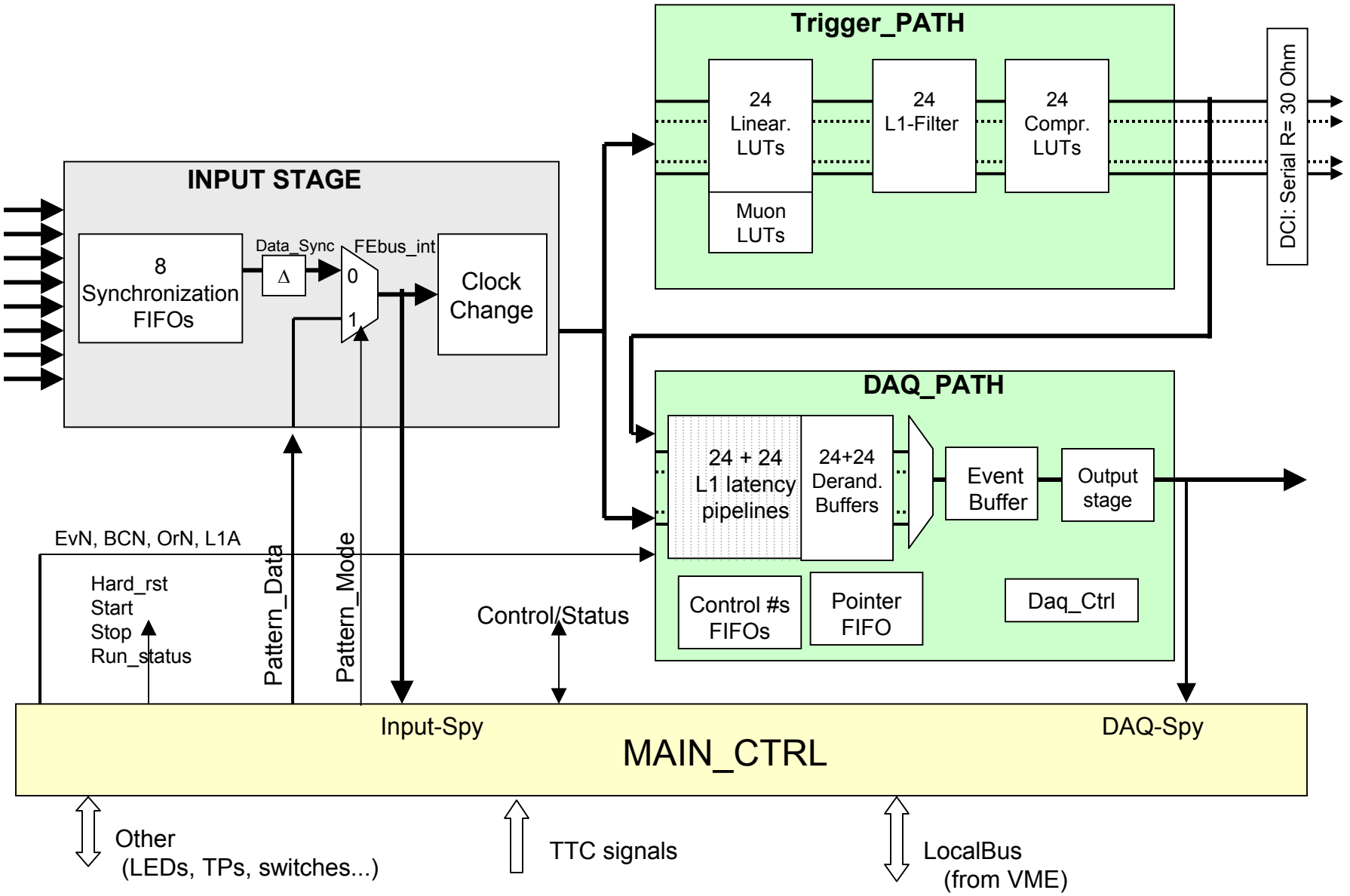
- Only components with a random latency are sketched -



Next pages contain details of the design.

They can be useful to interpret the HTR behaviour or FPGA code.

Main HTR FPGA – top level

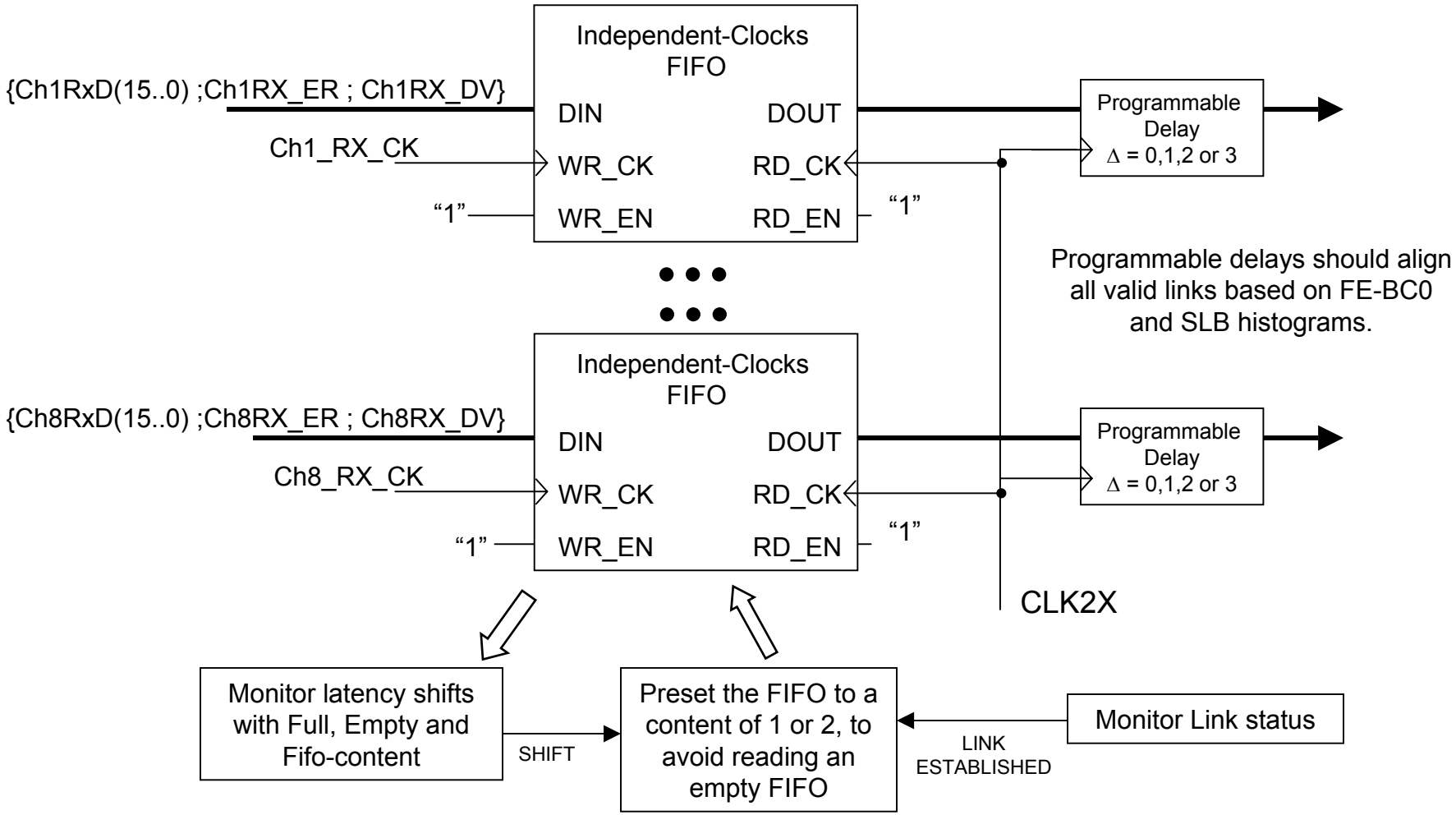


Synchronization FIFOs and Prog. Delays

Each incoming FE-bus is synchronous with its own Recovered_CK. This stage synchronizes the data to the System Clock x 2. Consider the “Self-Addressing” architecture for these FIFOs (improve timing uncertainties).

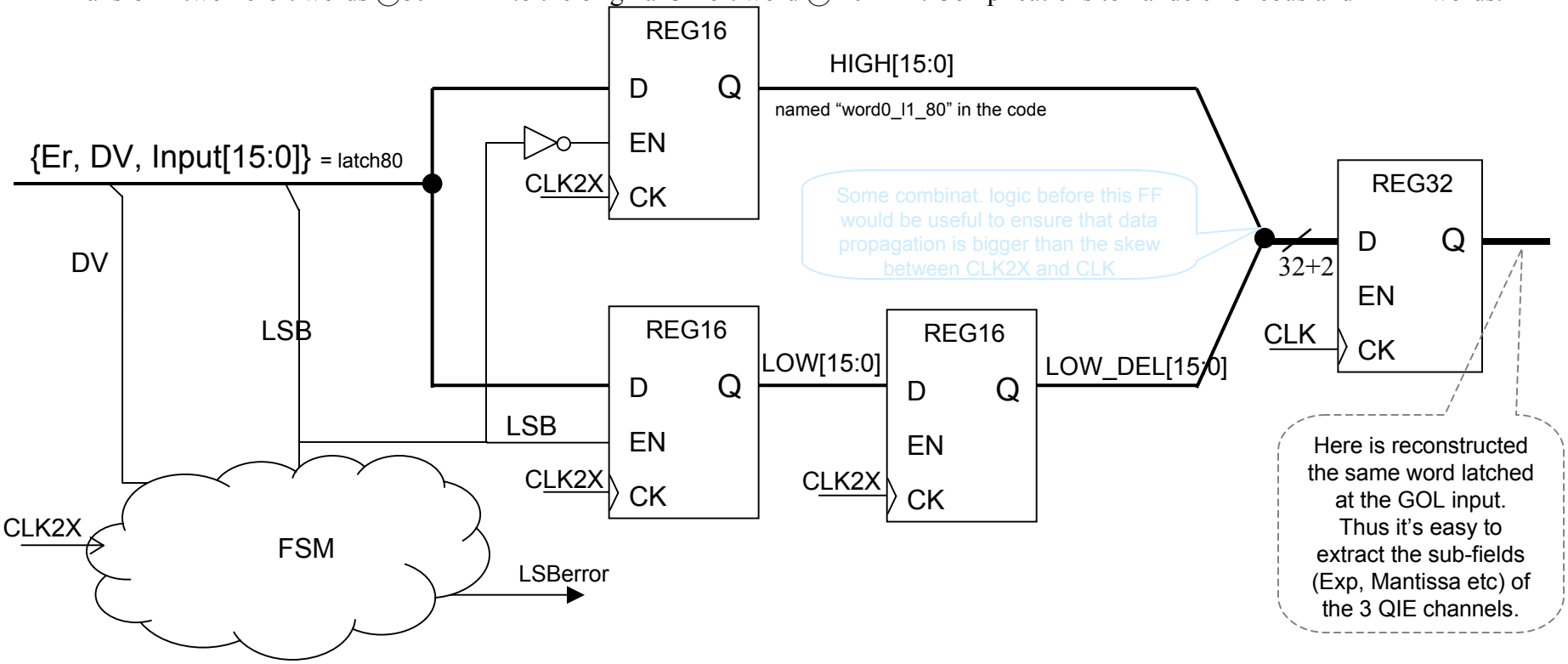
To align TPG data, a delay must be added to the corresponding channel. This value of each delay is the value of the gaps on the synchronization histogram. [Carlos].

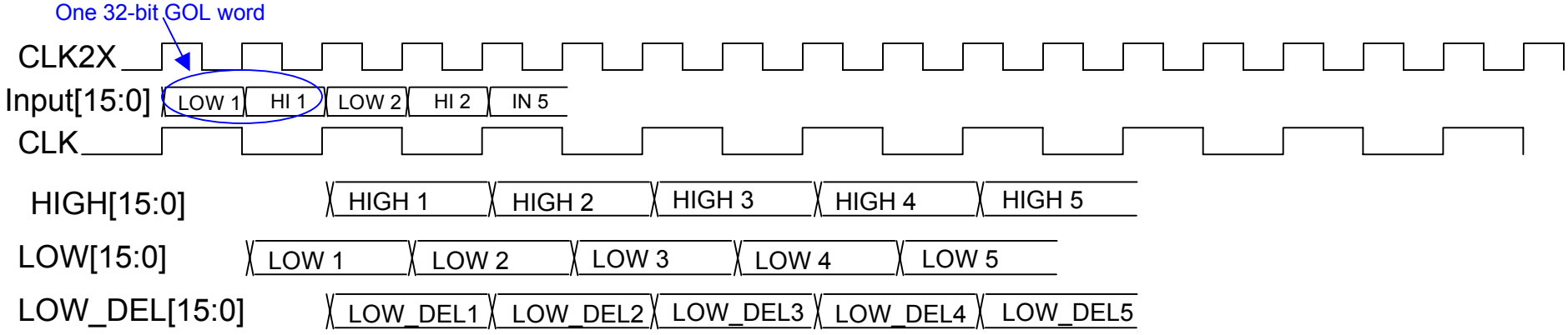
Make sure that when the link is down there is a free-running RX_CK from the TLK2501, in order to write ER and DV.



Clock Change stage (simplified)

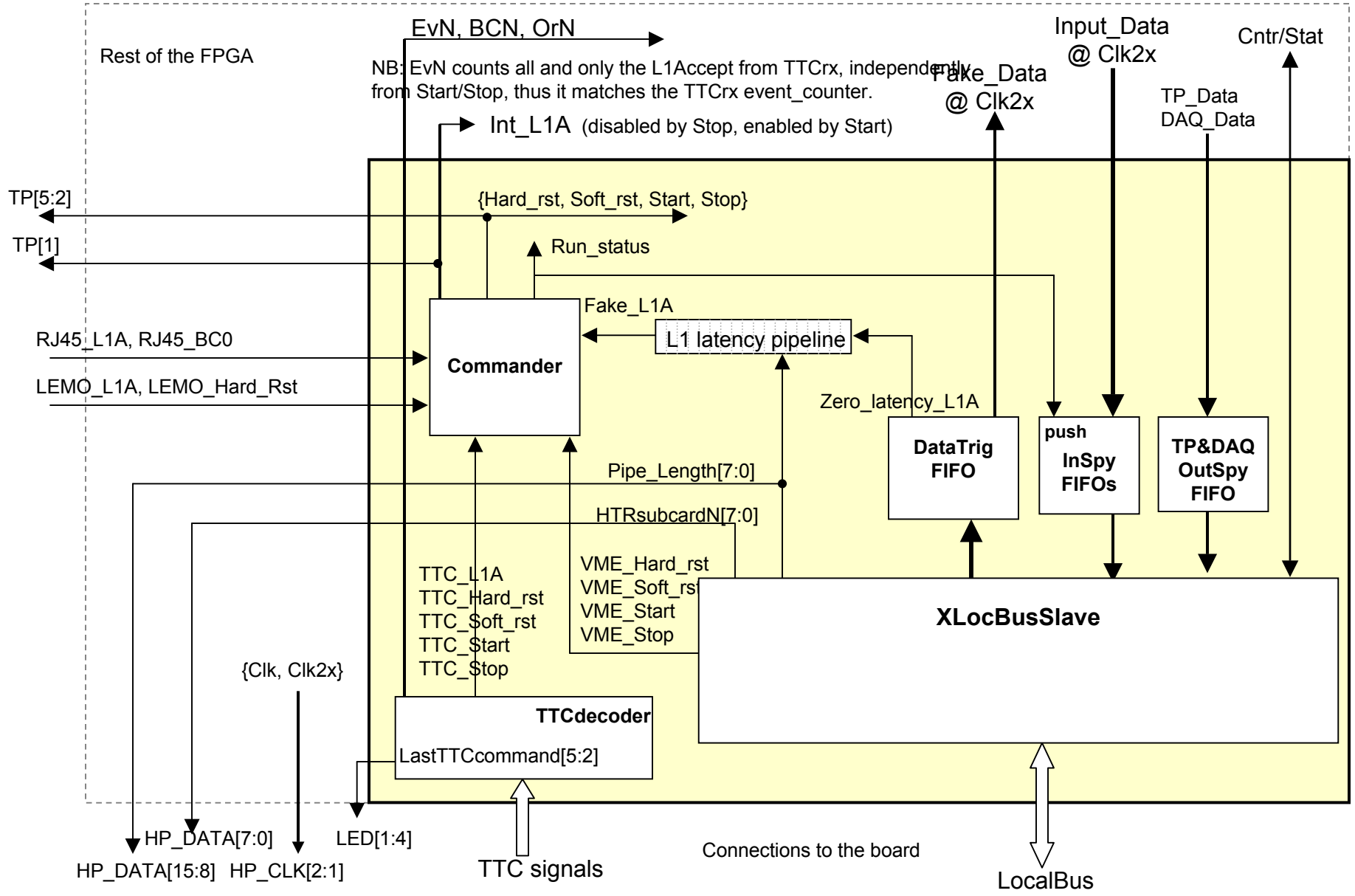
Transform two 16-bit words @80MHz into the original 32-bit word @ 40MHz. Complications to hande erroneous and IDLE words.





Control module of Main FPGA - MAIN_CNTR

TBD: "Resync" : command interpreted as a re-synchronization of all sub-systems readout to the same event. Event and bunch counters as well as readout memories and pointers are reset.



HCAL L1 (Trigger) Path - Proposal

The data coming from the front-end (QIE) are in the 7-bit Mantissa-Exponent format. They have a resolution of about 0.25 GeV and a maximum energy of 2714 GeV [CMS IN 2001/037, Fig.5]

The sequence of operations in the HCAL **T**rigger **P**rimitive **G**enerator (HTR board) is (see next pages) :

0) Reset the TP if any of the following: 32 bit-Link not OK; CapIDError; GOL_reconstructed_data[2:1] ≠ (0, 1); latency_shift ?

1) Linearize the data with a LUT on a 10-bit transverse energy value. If we assign the resolution = LSB = 0.5 GeV this gives an end-of-scale value of 512 GeV.

2) Apply a filter (still under study) for **B**unch **C**rossing **ID**entification. The filter will likely sum two consecutive time-samples and then perform a peak-detection (and maybe apply a threshold).

3) Sum 1 to 7 linearized channels of transverse energy. In case of overflow the output is set to the maximum.

4) The next step is the compression for the transmission of the **T**rigger **P**rimitives to the **R**egional **C**alorimeter **T**rigger. We use a LUT with 10-bit input.

5) The Muon window must be applied directly on the QIE-format, using a LUT with a 2-bit output, with the following meaning:
   - 00: energy below low-threshold
   - 01: energy within low-threshold and high-threshold
   - 10: energy bigger than high-threshold
   - 11: unused

6) The BCID information allow to select the 2-bit vector corresponding to the peak of the event (this avoids to flag as a muon the tail of a more energetic event).

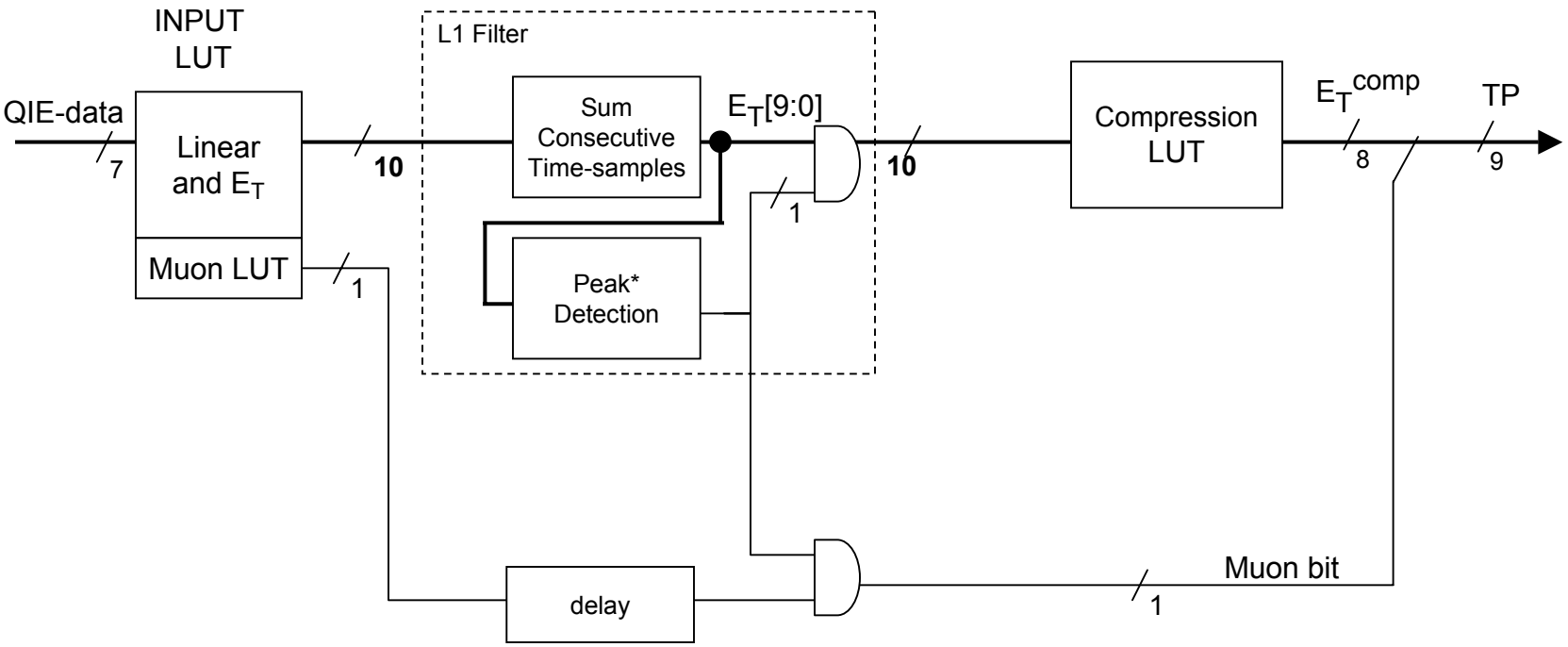
7) If there are multiple channels, the 2-bit vectors go into another LUT; this is to take care of cases where showers can leak into a cell and incorrectly set the muon bit: "If two muons are input, and both are below the low threshold or above the high threshold, then the output is 0. If both are above the low and below the high threshold, then the output is 1. If one is below the low threshold and one is above the low threshold _and_ below the high threshold, the output is 1. If one is above the high threshold, then the output is 0 irrespective of the value of the second." [W.Smith]

8) At least for HB/HE, try to make a firmware where a single"header" file can remap the way channels are added. All firmware versions will always have the worst-case (biggest) adders, with spare inputs. This header file should also control a sub-field of the FPGAversionNumber [from a discussion with Jeremy, MAR05]. even better if this is controlled by VME registers.

NOTES: HF analog pulse is faster than HB, HE, HO: no need for L1 energy filter.
HO HTR need to generate only one bit per channel, for RPC trigger.

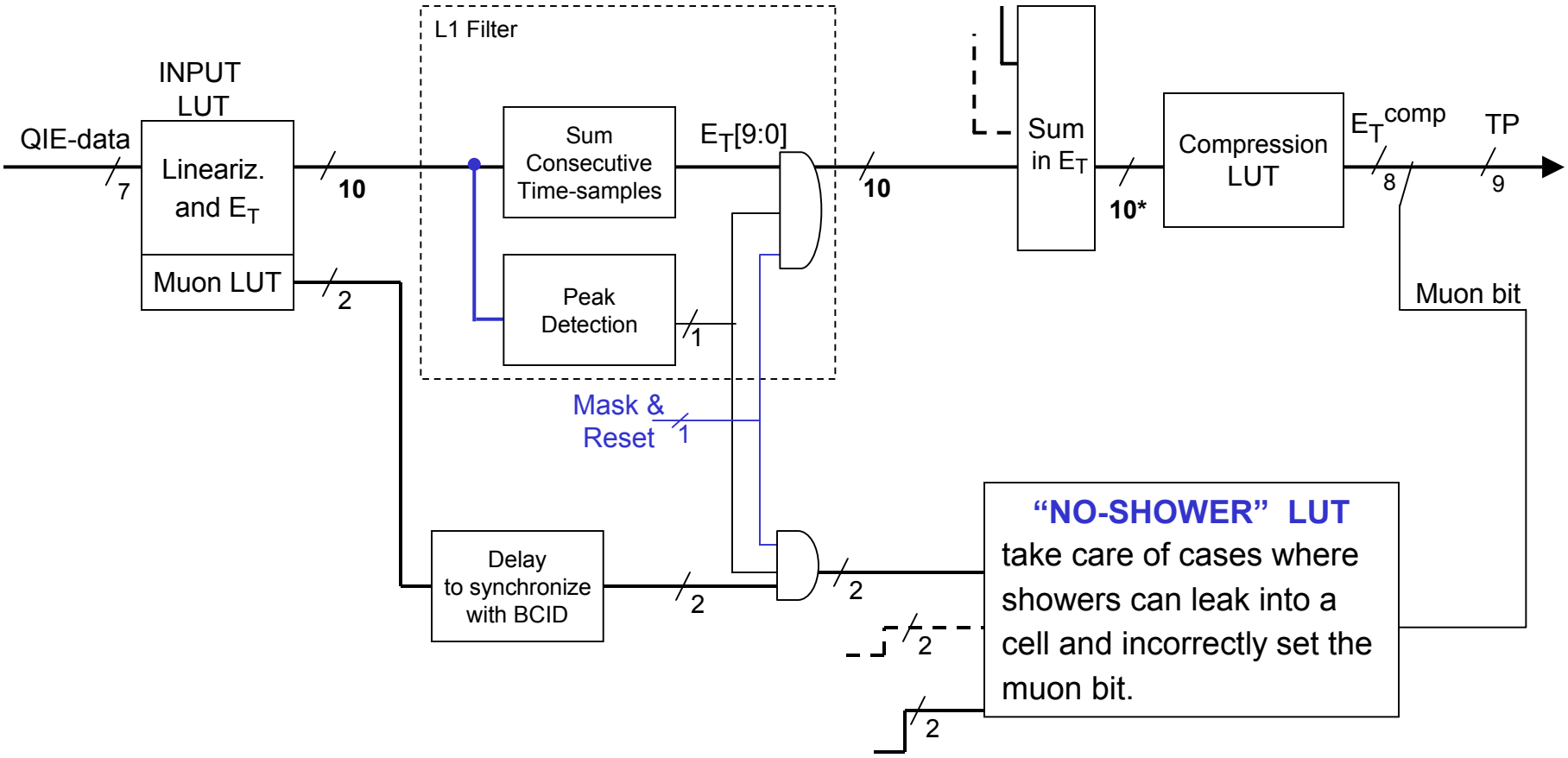
Trigger-Path
Case without Sum of QIE-channels

This scheme is simplified and it is correct in the nominal conditions. Features not shown:
- data are set to zero if any error is detected;
- the filter is by-passed if set by VME,
- the peak-detection can be disactivated over VME, only for the copy of the Trigger Primitives sent to the DAQ.



In case that after the summing there is a "plateau" [e.g.: 0, 10, 10, 0] select all the relative maximum points.
In HF the pulse is faster and there is no need to do the L1 filter.

New Trigger-Path : Sum n(<8) QIE-channels

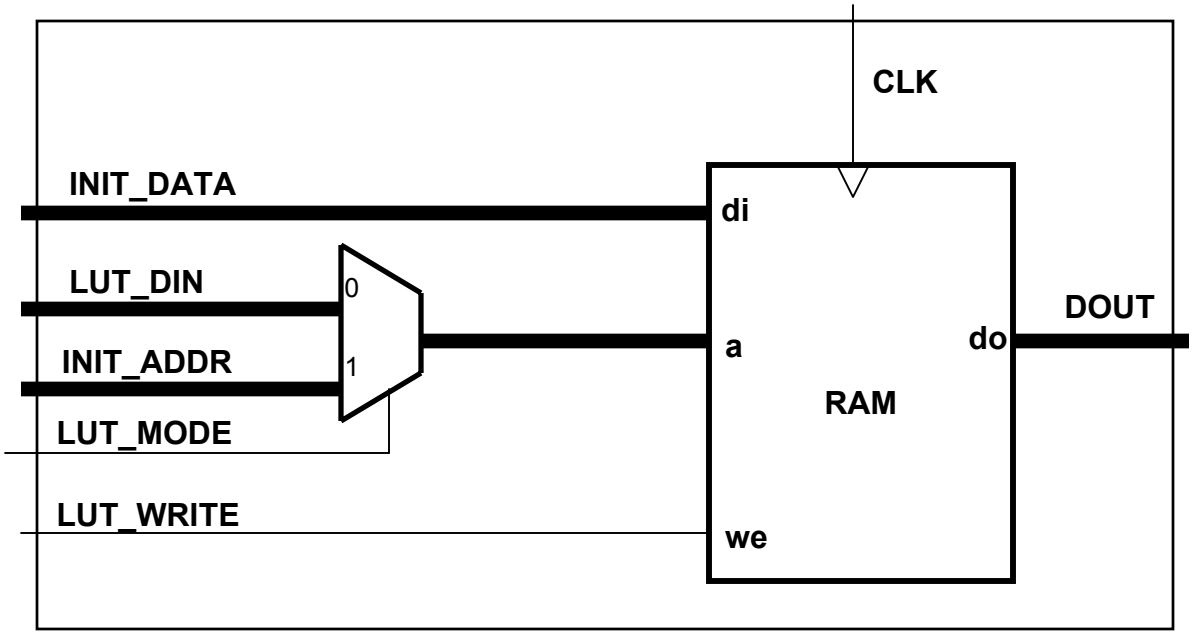


* If overflow, set the result to the max value.Investigate 11-bit sum and LUT. Note that there is a unique compression LUT for a group of channels.
Each channel participating on the sum must have the possibility to be masked, to perform a sync histogram based on each independent channel (input data from each deserialiser) [Carlos]
Doing the Peak-detection in parallel with the Sum decreases the latency, and it can be used to off-set the latency of the following sum of trigger towers.

HTR firmware customizations

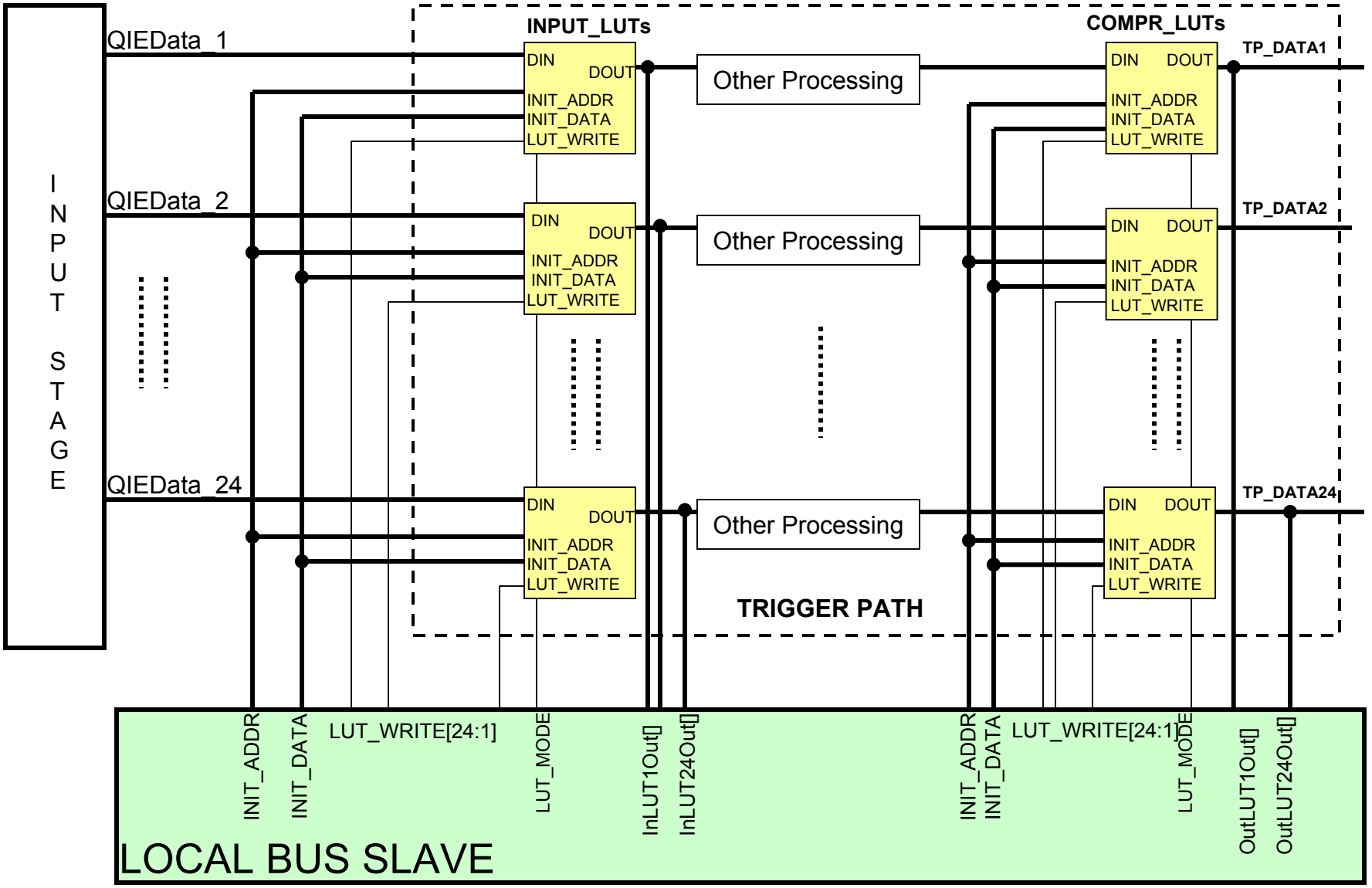
HO HTR need to generate only one bit per channel, for RPC trigger. Latency constraint ?
HF analog pulse is faster than HB, HE, HO, and it is completly contained in a 25ns sample: no need for L1 energy filter.
HF: luminosity output and jet triggers.

LUT Module



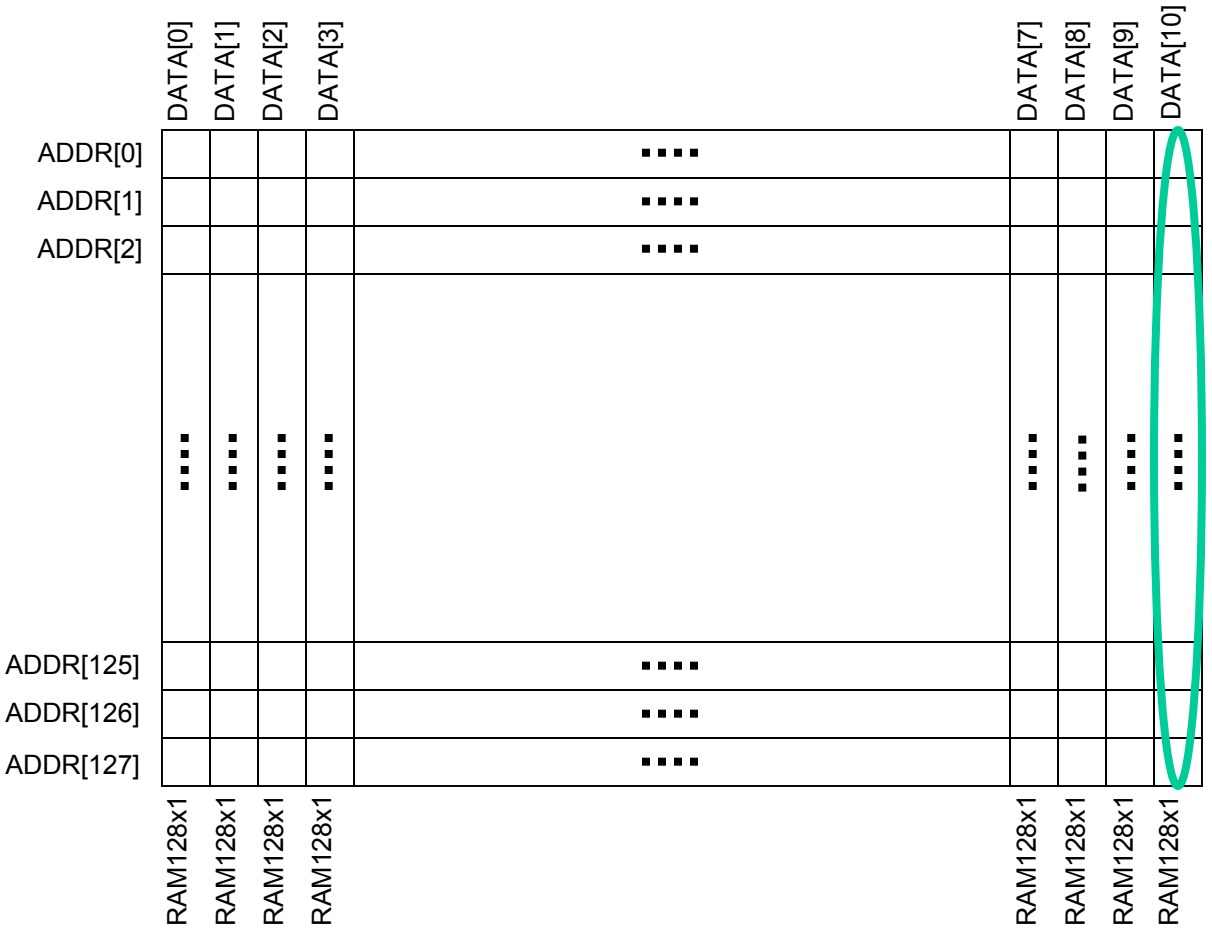
NB: during configuration this LUT has non-zero outputs, so need to disable (Stop command) the SLB board (software specification).
This is not done in this module in order to reduce the latency.

LUT Initialization Scheme over VME-Local Bus



NB: to configure a given LUT, from VME the access will be always at the same address. Then on the board VME FPGA the correct address will be generated with a counter.

Input LUT initialization at compilation time

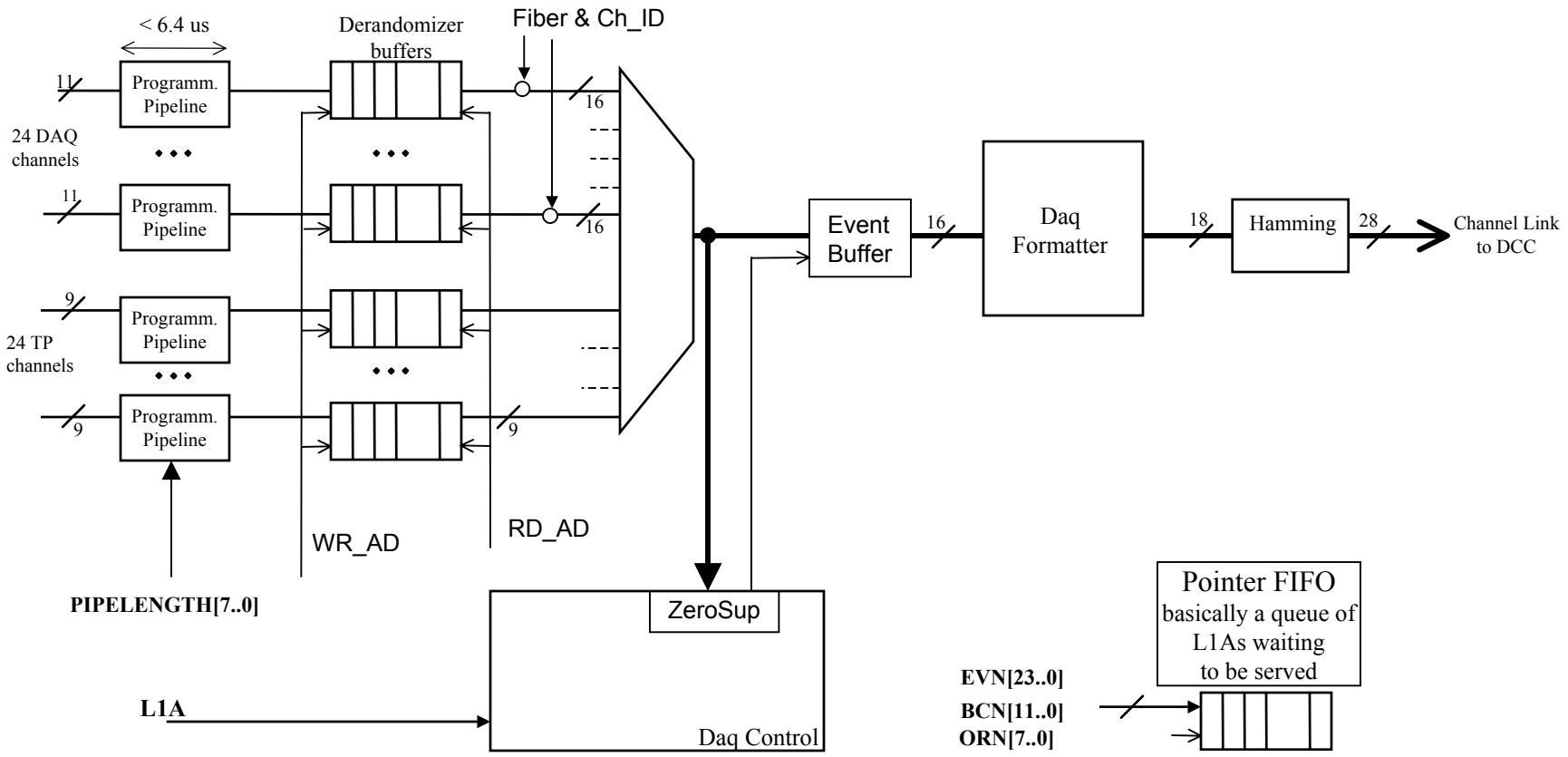


NOTE:
The Input LUTs in the Trigger Path use Single Port Distributed Ram. The 128x11 memory needed is mapped to 11 128x1 distributed ram primitives as shown in the figure.
The first bit of all 128 locations are mapped to one instance of the primitive, the second bit of all 128 locations are mapped to the second instance and so on. This information is needed when we need to initialize the ram contents at power up. The initial values can then be put in the UCF file accordingly. Each of the 11 instances have to be initialized separately.

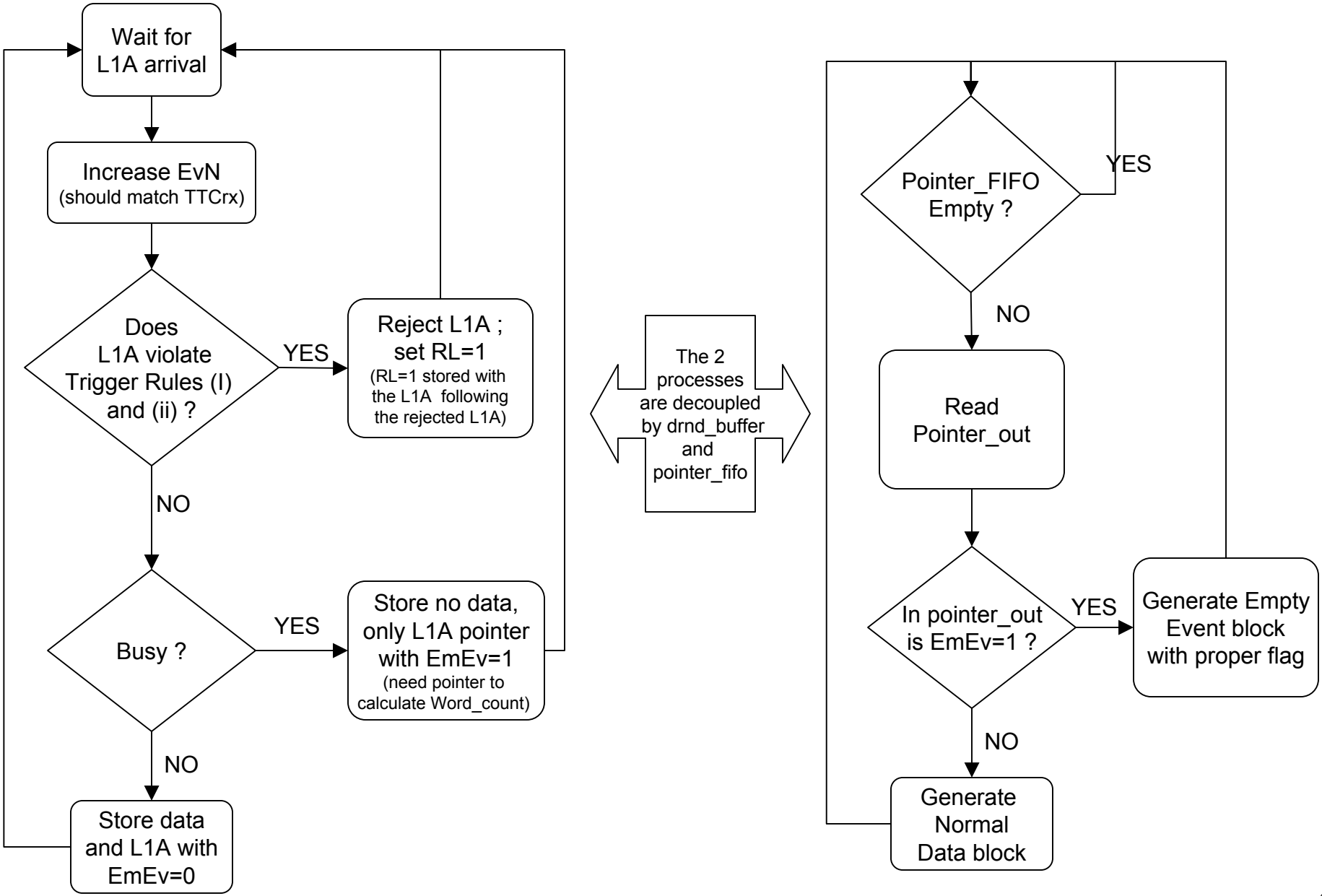
One 128x1 Distributed Ram Primitive

L2-DAQ Path

No energy extraction algorithm ⇒ QIE-data + address.
The 24 QIE-channels (in parallel with the 24 TP-channels) are temporarily stored in a pipeline (circular buffer) to wait for the L1A trigger decision. The storage time is programmable between 0 and 255 clock ticks. Each L1A trigger selects a block of time-samples per QIE-channel and energies per TP-channel. The selected data of the 24 channels must be inserted on the HTR/DCC data format. EV#, BC#, ORBIT# must correspond to the appropriate data.
Investigate how to align the DAQ-channels using SLB info.

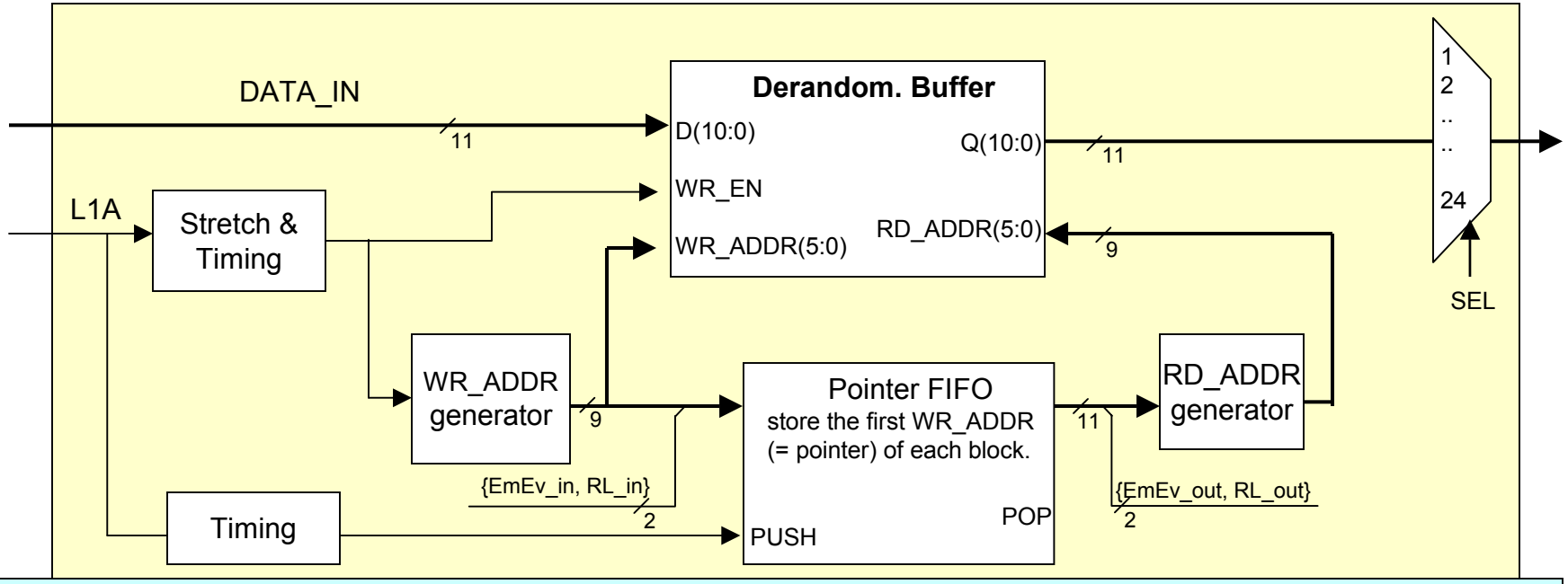


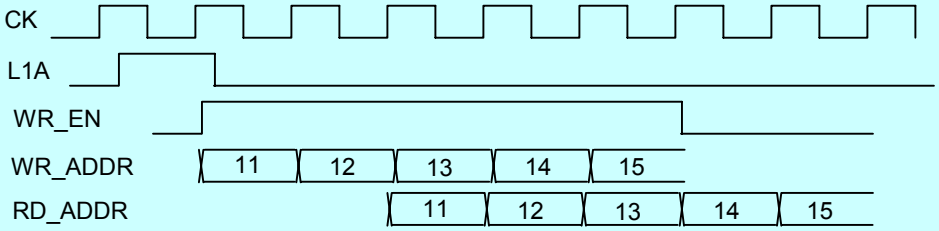
Trigger acceptance & Empty events



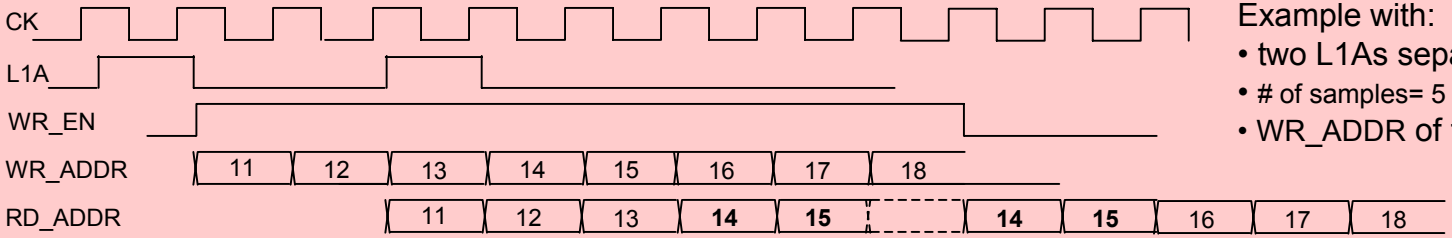
Derandomizer and trigger rules

The Derandomizer is not a simple FIFO as it handles the case of two L1A within a 4-tick interval (Trigger TDR 16.4.3). Such an interval is smaller then the number of time samples (≈ 10) to be collected (Trigger TDR 7.3.1), thus overlapping.





Example with:
- # of samples = 5
- WR_ADDR of the first word = 11

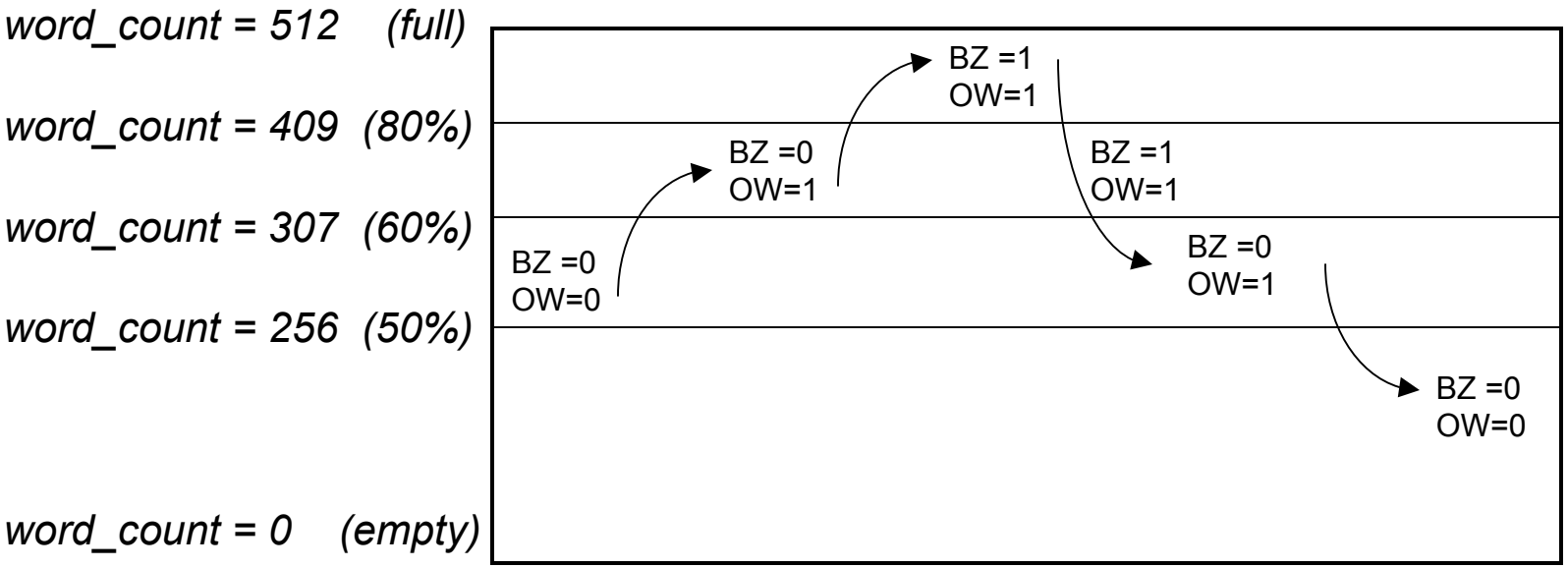


Example with:
- two L1As separated by two BXs
- # of samples= 5
- WR_ADDR of the first word = 11

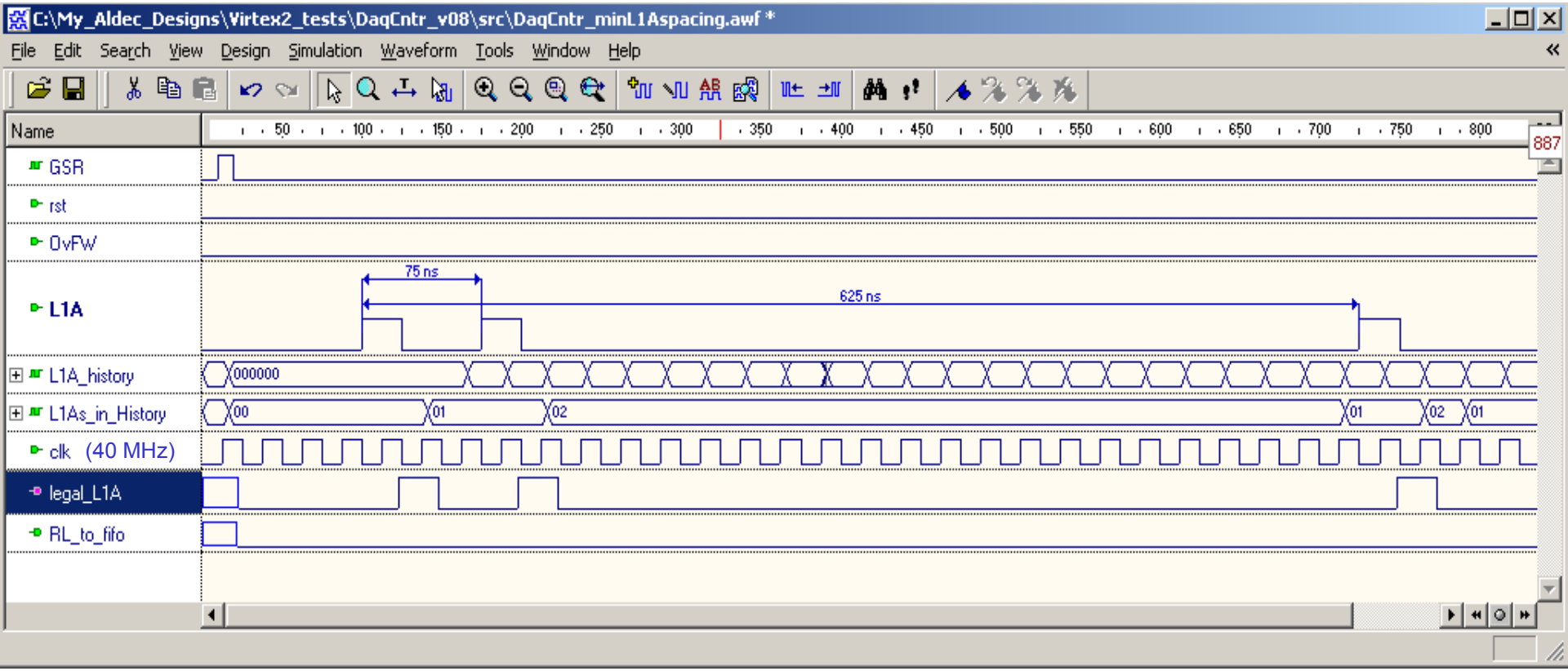
Overflow Warning (OW) and Busy (BZ) flags

Derandomizer buffers are Synchronous dp-Rams 36 X 512 deep. They are the first elements that can overflow in the HTR, in case of a high trigger rate.
Let: *word_count = drnd_wr_addr – drnd_rd_addr*

We introduces a sort of histeresys, to avoid that the flags keep toggling when the buffer are around a threshold:

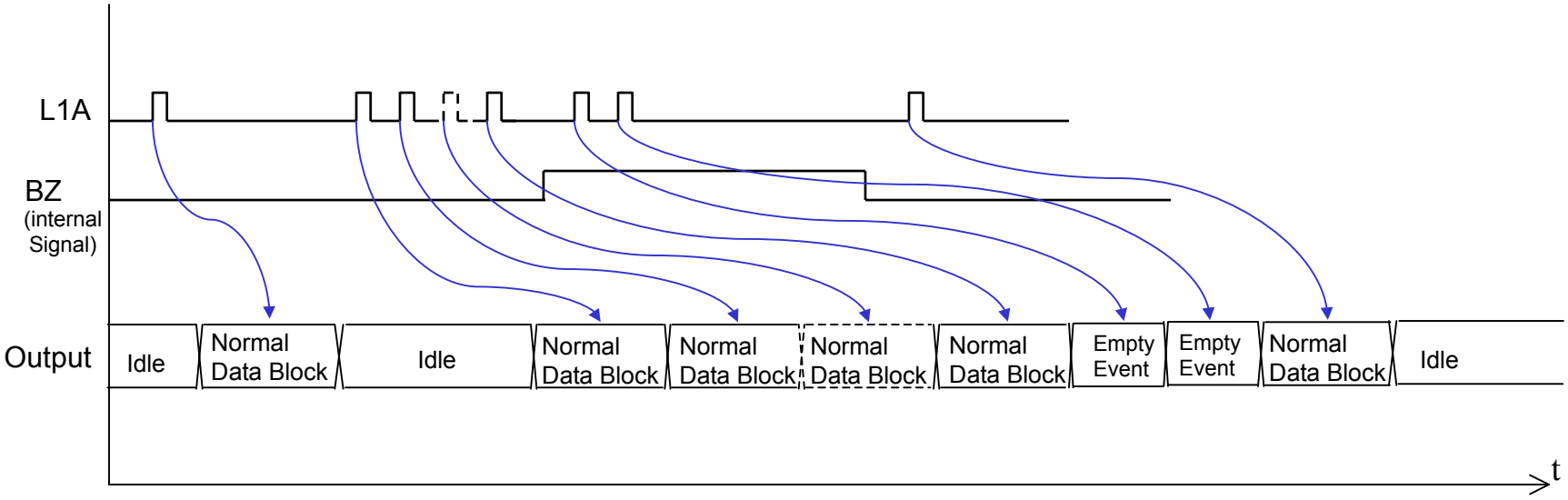


Example of minimum L1A spacing that does not violates the Trigger rules



Example of DAQ-output sequence

In this example there are no rejected L1As (i.e. Trigger Rules are not violated)



Note that the BZ included in each Data Block, latches the value of the internal BZ at the beginning of each block transmission.

Zero Suppression – from v25

Given that:

- DAQ-Data are time-sample, not energies
- Trigger Primitives are transverse energies.

  ⇒ zero-suppression based on a check on the Trigger Primitives, (the Primitive defined by the length of the L1A-latency-pipeline, “pipelength” parameter). This is fine to cut pile-up, but to cut noise we would really need a cut on energy (in future ?).

The firmware has two operating modes based on the parameter NS set over VME:

Normal CASE: $0 < NS \leq 10$

if E_T < DaqTh send 0 DAQ-samples,
else send NS DAQ-samples.

if E_T < TpTh send 1 Trigger Primitive,
else send NS Trigger Primitives.

Debugging CASE: $10 < NS < 21$

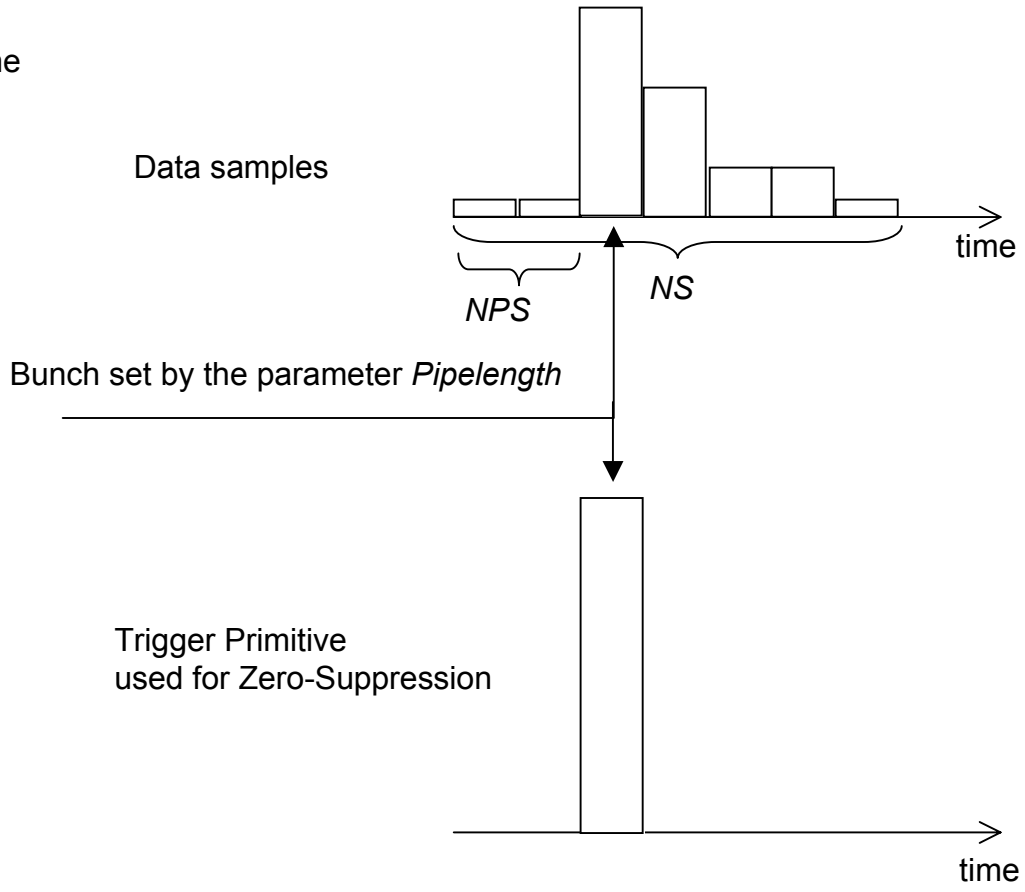
if E_T < DaqTh send 0 DAQ-samples,
else send NS DAQ-samples.

Send exactly 1 Trigger Primitive.

The thresholds DaqTh and TpTh are set over VME individually, per channel.
They are 9-bit values applied on compressed E_T (an 8-bit value), so we can set a threshold high enough to always suppress.
Setting a threshold to 0 implies all the words pass.

Alignement of Data and trigger Primitives in the DAQ-Path – not implemented

NS = Number of Samples, set over VME
NPS = Number of Pre-Samples, set over VME
The Trigger Primitive must always correspond to the energy of $sample_{NPS+1}$ + $sample_{NPS+2}$.



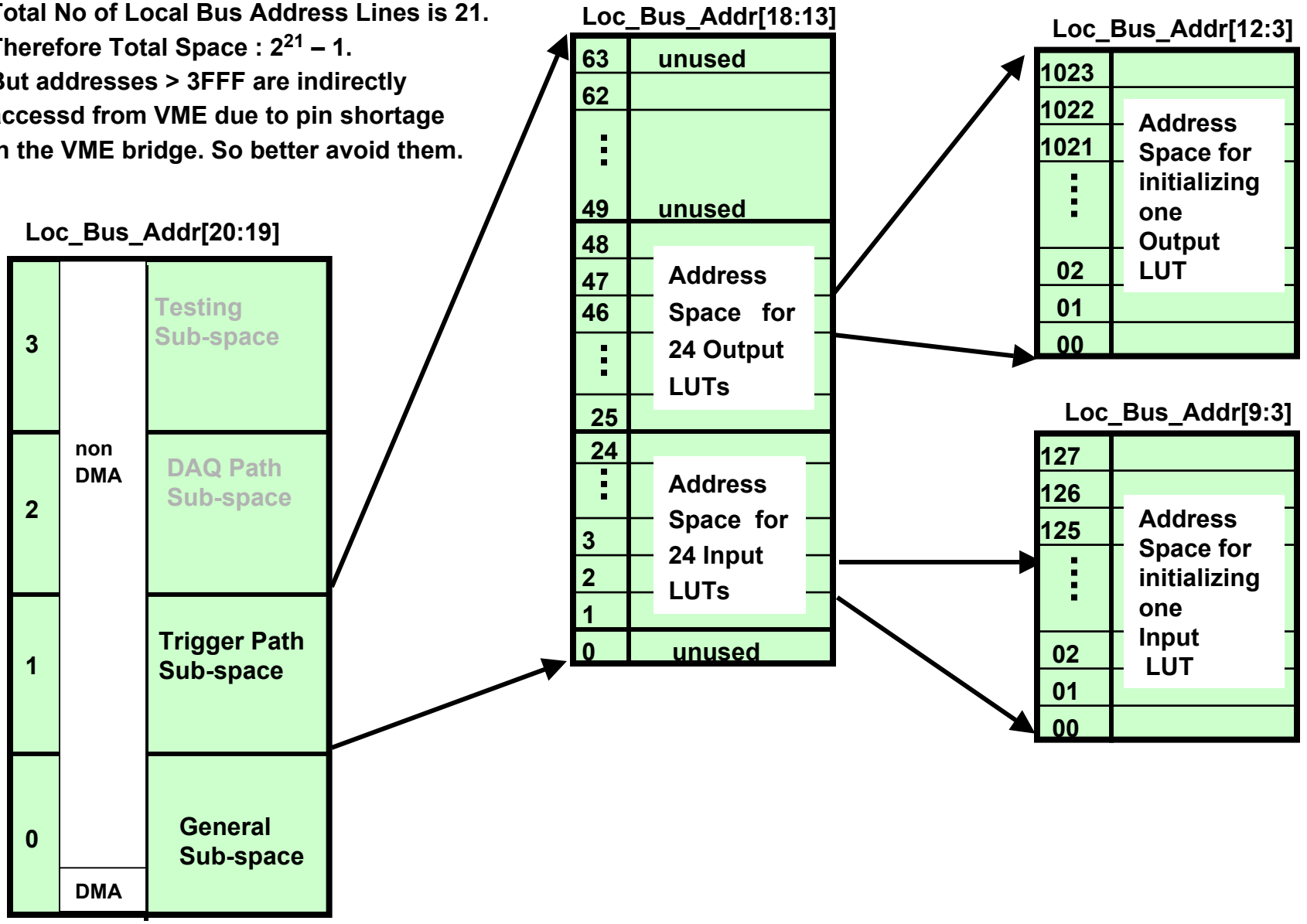
Pedestal calculation

Study the possibility to calculate the pedestal as an average of the input value during the abort gap. For instance accumulate 32 inputs and then divide by 32 (simple shift).
If the abort gap is used for something else (IDLE patterns, etc), calculate the pedestal taking data during the minor gaps (~38 BXs). For instance accumulate the 16 inputs and then divide by 16 (simple shift); this protects from random latency effects, etc.
This must be done per channel.
Pedestal values should be sent out to the DCC and/or used for zero suppression and energy filtering.

Address Section

Details on http://www.physics.umd.edu/hep/HTR/preprod/Xilinx_addr_map.html

Total No of Local Bus Address Lines is 21.
Therefore Total Space : $2^{21} - 1$.
But addresses > 3FFF are indirectly accessd from VME due to pin shortage in the VME bridge. So better avoid them.



HTR-DCC Data Format - (output of the HTR DAQ-path up to HTRev4_v9)

Word Type	S1 S0	Byte 1	Byte 0
HEADER	1 1	Zeroes	EvN [7:0]
Ext. Header2	1 0	EvN [23:16]	EvN [15:8]
Ext. Header3	1 0	PipeLength[7:0]	HS | RL | EE | SR | BZ | OV | HM | TM
Ext. Header4	1 0	OrN [7:0]	HTR_sub_module_Number
Ext. Header5	1 0	BCN[11:8]	BCN [7:0]
Ext. Header6	1 0	Total number of TP words[7:0]	TrigType[3:0] | DLL_unlock[2:0] | TTCready
TP-DATA1	1 0	{FiberAd[2:0];ChAd[1:0]; 0; PS; TP[8:0]}	
…	1 0	…	
TP-DATAm	1 0	{FiberAd[2:0];ChAd[1:0]; 0; PS; TP[8:0]}	
DAQ-DATA1	1 0	{FiberAd[2:0]; QIEAd[1:0]; Er; DV; CapID[1:0],QIEData[6:0] }	
…		…	
DAQ-DATAn	1 0	{FiberAd[2:0]; QIEAd[1:0]; Er; DV; CapID[1:0],QIEData[6:0] }	
Extra-Info1	1 0	Arrival time (BCN) of Bzero from Fiber1 [11:0] (to study the latency) or other info	
	1 0	Arrival time (BCN) of Bzero from Fiber2 [11:0] (to study the latency) or other info	
	1 0	Arrival time (BCN) of Bzero from Fiber3 [11:0] (to study the latency) or other info	
	1 0	Arrival time (BCN) of Bzero from Fiber4 [11:0] (to study the latency) or other info	
	1 0	Arrival time (BCN) of Bzero from Fiber5 [11:0] (to study the latency) or other info	
	1 0	Arrival time (BCN) of Bzero from Fiber6 [11:0] (to study the latency) or other info	
	1 0	Arrival time (BCN) of Bzero from Fiber7 [11:0] (to study the latency) or other info	
Extra-Info8	1 0	Arrival time (BCN) of Bzero from Fiber8 [11:0] (to study the latency) or other info	
	1 0	NDD = # of Daq-Data samples (per L1A)	NTP = # of TPs (per L1A)
	1 0	WordCount[11:0]	
Pre-Trailer	1 0	Zeroes	Zeroes
TRAILER	0 1	EvN [7:0]	Zeroes

n = # of DAQ-DATA words ≤ 24x20 (depends on Zero-suppression). NB: the number of words with [S1 S0] = [1 0] must be a multiple of 2.
TM = Test Modes: can be CounterMode or PatternMode: if "0" real data; if "1" test data. Trigger needed as in the real mode. Set from VME.
HM = Histogramming mode, need to change firmware to switch. **OV**= Overflow. For debugging purposes (it should never happen).
BZ = Busy. It should be reported to the aTTS by the DCC. **SR** = Status Request (from a TTC command, for the DCC LRB)
EE = Empty Event (consequence of a past BZ). An **Empty Event** includes only the first 5 header words and the last 3 words.
RL = Rejected previous L1A (when previous L1A violates the trigger rules i and ii of Trigger TDR 16.4.3)
HS = when in Histogramming mode, indicates which Set of fibers are used: when this bit is 0, histograms are from fibers 1-4 .
TrigType: if (TTC_L1A) trig_type <= 1; if (VME_L1A) trig_type <= 2 **PS** = PatternSelected from RAMs upon TTC_TestEn
EvN = TTCrx EvN **DLL_unlock[2:0]** = count of how many times the DLL unlocked since last Hard_rst