

Poly(3-hexylthiophene) thin-film transistors with variable polymer dielectrics for transfer-printed flexible electronics

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The fabrication of high quality organic thin-film transistors onto flexible, plastic substrates has been extended to include the polymeric semiconductor material poly(3-hexylthiophene). The transfer printing method is used to easily assemble these devices onto either polyethylene terephthalate (PET) or polycarbonate (PC) substrates. A PC dielectric layer is used in conjunction with the PC substrate while both poly(methyl methacrylate) and polystyrene dielectric layers are used in conjunction with the PET substrate. In all cases the mobility of the transfer-printed devices, $0.019\text{--}0.041\text{ cm}^2/\text{V s}$, is significantly higher than that of the unprinted reference devices (SiO_2 dielectric layer on a Si substrate), $0.007\text{ cm}^2/\text{V s}$. The width-normalized contact resistance is also lower for the transfer-printed devices, $0.18\text{ M}\Omega\text{ cm}$, as compared to that for the reference devices, $0.56\text{ M}\Omega\text{ cm}$. For the devices reported, the threshold voltage becomes more positive as the polar component of the surface energy of the polymer dielectric material increases. These results illustrate the simplicity, power, and versatility of the transfer printing method for the fabrication of high quality flexible electronics. © 2008 American Institute of Physics. [DOI: 10.1063/1.2959821]

I. INTRODUCTION

Advances in flexible electronics require simple, high-volume fabrication methods that can produce high quality devices.^{1–3} Plastics are an attractive substrate and dielectric material for numerous reasons such as the ability to tune physical properties, as well as low cost, light weight, optical clarity, compatibility with roll-to-roll processing, etc. Transfer printing^{4–10} methods have been developed for the assembly of organic thin-film transistors (OTFTs) onto plastic substrates where no mixed processing is performed on the device substrate (i.e., all device components are printed onto the plastic substrate in exactly the same way).^{11,12}

The transfer printing process has been demonstrated for pentacene (Pn),^{11,12} poly(3-hexylthiophene) (P3HT),^{11,13} carbon nanotube networks,^{14–21} and graphene²² as active semiconductor layers, with poly(methyl methacrylate) (PMMA) as the gate dielectric. The process has been optimized for Pn devices, where it has been shown that, due to the laminated contacts and thermal annealing of the organic semiconductor, the OTFT devices printed onto plastic perform better than comparable unprinted devices on an inorganic substrate with evaporated top contact source and drain (S/D) electrodes.^{12,23}

Because transfer printing relies primarily on differential adhesion, this technique can be used to incorporate a wide variety of materials into printed electronics. Here, the transfer printing technique is extended to a variety of gate dielectric materials to create high quality OTFT devices using P3HT as the active semiconductor layer. The device/

substrate combinations studied are (1) a PMMA dielectric and polyethylene terephthalate (PET) (Dupont Mulinex 453/700) substrate (hereafter referred to as P3HT/PMMA/PET), which is similar to our previously reported Pn devices,¹² (2) a polystyrene (PS) dielectric and PET substrate (P3HT/PS/PET), and (3) a polycarbonate (PC) dielectric and PC (Bayer Tekra DE1-1D Makrofol 0.007) substrate (P3HT/PC/PC). The performance of the flexible P3HT devices fabricated with these different dielectrics is compared to the performance of unprinted reference devices fabricated on Si substrates with a SiO_2 dielectric layer (P3HT/ SiO_2 /Si). In all cases the mobility of the transfer-printed devices, $0.019\text{--}0.041\text{ cm}^2/\text{V s}$, is significantly higher than that of the unprinted reference devices, $0.007\text{ cm}^2/\text{V s}$. The width-normalized contact resistance is also lower for the transfer-printed devices, $0.18\text{ M}\Omega\text{ cm}$, as compared to that for the reference devices, $0.56\text{ M}\Omega\text{ cm}$. For the devices reported, the threshold voltage becomes more positive as the polar component of the surface energy of the polymer dielectric material increases, indicating that the threshold voltage can be tuned systematically through the dielectric choice. The three dielectric materials used have different polarizabilities, dielectric constants, and adhesive properties; hence our successful demonstration of device fabrication with these materials highlights the compatibility of the transfer printing method with a wide range of material combinations.

II. FABRICATION OF REFERENCE DEVICES

Research on OTFTs is most commonly carried out with the organic material deposited onto a thermally oxidized,

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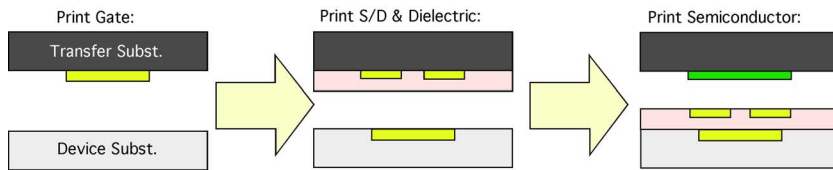


FIG. 1. (Color online) Illustration of the transfer printing method for the fabrication of bottom gate/bottom S/D OTFT devices onto flexible substrates.

doped Si substrate (SiO_2/Si), with the SiO_2 used as the dielectric layer and the Si substrate as a global gate electrode.^{24–27} S/D electrodes are typically deposited either before (bottom contact) or after (top contacts) the organic layer. Such bottom contact devices are fabricated here for use as reference devices. The S/D contacts were patterned using standard photolithography with a 10 Å thick chromium wetting layer, a 100 nm thick gold layer, channel lengths $L=3\text{--}1300\text{ }\mu\text{m}$, and channel width $W=2000\text{ }\mu\text{m}$. Following lift-off the substrate and electrodes were rinsed with semiconductor grade acetone, methanol, and isopropanol alcohol and dried with nitrogen. The semiconducting layer was formed by spin casting 94.5% regioregular P3HT ($M_n=13\,000$ and $M_w=26\,200\text{ g/mole}$, Merck) dissolved in chloroform (>98%, Aldrich) at a concentration of 0.5 mg/ml after being passed through a 0.2 μm polytetrafluoroethylene (Teflon) (PTFE) filter. Spin casting was done under ambient conditions at a speed of 1250 rpm, with 1000 rpm/s acceleration, for 60 s, followed by a 2 min bake at 80 °C. The resulting P3HT film thickness was approximately 20 nm. Devices were kept inside a nitrogen glove box until electrical characterization was performed under a separate N_2 atmosphere on a Cascade probe station. While mounted on the Cascade probe station, a subset of the measured reference devices was annealed to 100 °C for several minutes. These annealed reference devices performed the same as the unannealed reference devices.

III. FABRICATION OF FLEXIBLE DEVICES

The transfer printing process used to fabricate P3HT OTFT devices on plastic substrates has been presented in detail elsewhere.¹² Here we will review the basics and discuss the details relevant to the P3HT devices. The model system for transfer printing OTFT devices onto plastic substrates has been developed using Au gate and S/D electrodes separated by a polymer dielectric layer on a thermoplastic substrate (the device substrate), as illustrated in Fig. 1. The electrodes were fabricated using photolithography on Si substrates (the transfer substrate). To improve adhesion of the Au electrodes to both the thermoplastic device substrates and to the polymer dielectric layers, the electrodes were exposed to a 200 W, 19 SCCM (SCCM denotes cubic centimeter per minute at STP), 250 mTorr O_2 plasma for 5 min in a PlasmaTherm 790. In order to lower the adhesion between the device and transfer substrates for printing of the gate electrodes, a treatment of the SiO_2 surface was used as follows. The gate electrode was first treated with benzyl mercaptan for 2 h to protect the Au surface. The release layer (tridecafluoro-1,1,2,2-tetrahydro-octyl) trichlorosilane was then applied to the transfer substrate surface. Both treatments were performed in a custom vapor deposition chamber. The

gate electrodes were printed directly to the device substrate at an imprint pressure of 500 psi while held at 170 °C for 3 min.

For printing of the S/D electrodes, the polymer dielectric layer was spin coated onto the transfer substrate containing the S/D electrodes. Each polymer dielectric layer required different processing conditions. For the PMMA dielectric layer, adhesion to the transfer substrate was a problem, so the S/D electrodes and transfer substrate were treated as described for the gate electrodes. The PMMA [molecular weight (MW) of 950 000, 7% solution in anisole; MicroChem Corp.] was spin coated at 2500 rpm for 60 s, baked on a hot plate at 90 °C for 3 min, and printed at 500 psi, 170 °C for 3 min.

For both the PS and PC (dielectric layers), adhesion to the transfer substrate was not a problem, so the S/D electrodes and transfer substrates were untreated prior to spin coating the polymer. PS (MW of 40 000, 7% solution in toluene; Sigma Aldrich) was filtered with a 0.2 μm filter, spin coated at 2500 rpm for 60 s, baked on a hot plate at 90 °C for 3 min, and printed at 500 psi, 170 °C for 3 min. The PC (MW of 39 000 g/mole, GE Lexan 1300) was typically dissolved to a concentration of 10 wt % in cyclohexanone. The solution was heated to 90 °C, filtered with a 0.2 μm filter, spin coated at 2500 rpm for 60 s, baked on a hot plate at 90 °C for 3 min, and printed at 500 psi, 150 °C for 3 min. For convenience and comparison, the parameters associated with printing of the S/D and dielectric layers are listed in Table I.

The P3HT films to be printed were prepared on a transfer substrate as discussed above for the fabrication of the reference devices except for the application of an octyltrichlorosilane (OTS) release layer prior to spin casting of the P3HT. The OTS layer was applied by soaking clean Si/ SiO_2 substrates in a $\sim 1\text{ mM}$ solution of OTS in hexadecane for 18 h in an oxygen- and moisture-free, nitrogen-purged glove box. Prior to printing, the transfer substrate was cleaved into $\sim 1\text{ cm}$ square pieces and the P3HT films were patterned manually into 3 mm squares using a fine tipped cleanroom swab. Finally, the patterned organic semiconductor film was printed onto the device substrate containing the previously printed electrode subassembly. The printing conditions of 600 psi and 100 °C for 3 min for the patterned P3HT layer were the same for all devices.

IV. DEVICE CHARACTERIZATION

To obtain the device capacitance, for each polymer dielectric layer a 3 mm \times 200 μm capacitor was fabricated by replacing the S/D electrodes by an electrode with a 3 mm \times 200 μm feature that overlapped an identical area of a gate

TABLE I. Device and fabrication parameters associated with the S/D electrodes and polymer dielectric layers.

Properties of S/D electrodes and polymer dielectric layer	P3HT/PMMA/PET	P3HT/PS/PET	P3HT/PC/PC
Electrode thickness (nm)	45	45	45
Electrode surface treatment	O ₂ plasma and benzyl mercaptan SAM	O ₂ plasma	O ₂ plasma
Transfer substrate surface treatment	Release layer SAM	None	None
Polymer/solvent	7%, 950 000 PMMA in anisole	7%, 40 000 PS in toluene	10% PC in cyclohexanone
Polymer spin coating	2500 rpm for 60 s, baked at 90 °C for 3 min	2500 rpm for 60 s, baked at 110 °C for 3 min	2500 rpm for 60 s, baked at 90 °C for 3 min
Polymer thickness (prior to printing) (nm)	960	720	460
Printing conditions	500 psi, 170 °C, 3 min	500 psi, 170 °C, 3 min	500 psi, 150 °C, 3 min
Dielectric layer capacitance (nF/cm ²)	4	3.2	6.3
Dielectric constant of dielectric layer	3.9	2.5	3.0
Surface energy of dielectric layer (mJ/cm ²)	39.86	29.7	29.96

electrode. For each capacitor, the capacitance was measured using a BK Precision 820 capacitance meter. The obtained values are listed in Table I.

Sets of devices similar to that shown in Fig. 2 were fabricated for each different dielectric material with channel length L ranging from 3 to 45 μm . The output and transfer characteristics of a P3HT/PMMA/PET device with $L = 15 \mu\text{m}$ and $W = 100 \mu\text{m}$ are shown in Figs. 3(a) and 3(b), respectively. The data in Fig. 3 are qualitatively similar to data for all the P3HT/PMMA/PET, P3HT/PS/PET, and P3HT/PC/PC devices. The linear region of the output characteristics was fitted to a straight line in the region from the S/D voltage $V_d = -5$ to -15 V for gate voltages $V_g = -20$ to -60 V. The slopes of these linear fits represent the total resistance (contact resistance + P3HT channel resistance) and are plotted (for the device shown in Fig. 3) in Fig. 4 as a

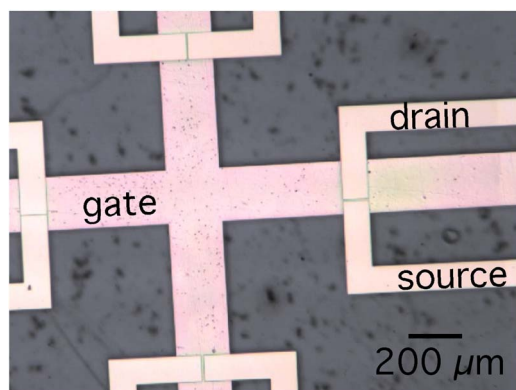


FIG. 2. (Color online) Optical image of transfer-printed OTFTs on a plastic (PET) substrate. For these devices, Au S/D and gate electrodes are separated by a 600 μm thick PMMA dielectric layer. Starting at the left and moving clockwise, the four devices shown here have channel lengths of $L = 1, 3, 6$, and 9 μm and a width $W = 100 \mu\text{m}$.

function of channel length (L) for each gate voltage. From such graphs, the contact resistances can be determined by extrapolating the resistance curves to $L = 0$ and the mobility (corrected for contact resistance) can be determined from the

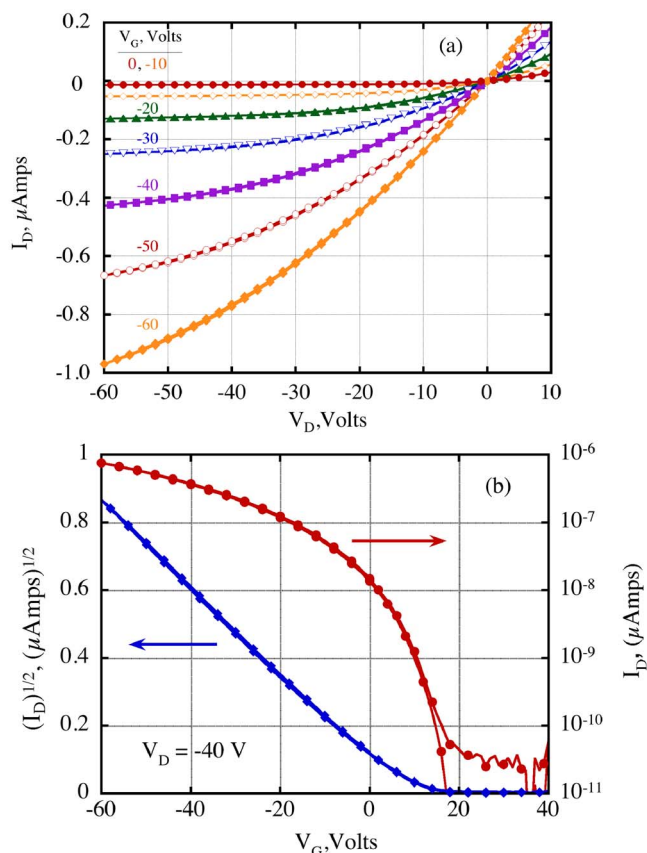


FIG. 3. (Color online) (a) Output characteristics of P3HT/PMMA/PET flexible OTFT with channel length $L = 15 \mu\text{m}$ and channel width $W = 100 \mu\text{m}$. (b) Transfer characteristics of device in (a).

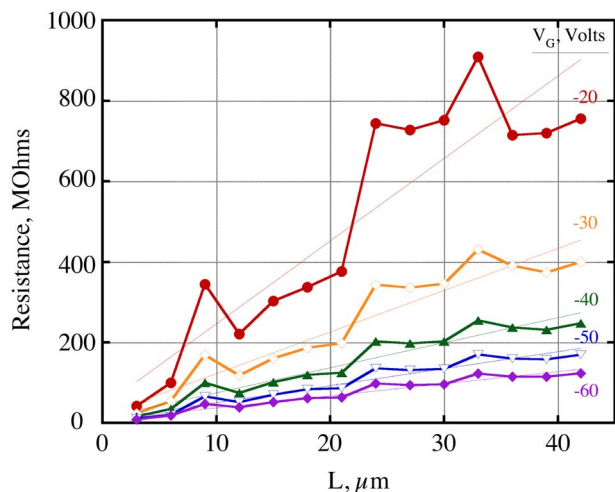


FIG. 4. (Color online) Resistance vs channel length for the set of transfer-printed P3HT/PMMA/PET flexible OTFTs at various gate voltages (symbols). Lines are linear fits used to extract the channel resistance per length (slope) and contact resistance (intercept).

equation²⁸

$$\frac{\partial[(dR_{\text{on}}/dL)^{-1}]}{\partial V_G} = \mu(V_G, T)WC_{\text{gate}}, \quad (1)$$

where C_{gate} is the capacitance of the gate dielectric. The contact resistance, mobility, threshold voltage, and on/off ratio for the P3HT/SiO₂/Si reference devices and the P3HT/PMMA/PET, P3HT/PS/PET, and P3HT/PC/PC flexible devices are tabulated in Table II.

V. DISCUSSION OF RESULTS

As is evident in Table II, the width-normalized contact resistance determined for the three flexible device sets is noticeably lower than that for the reference device set. This implies a better metal/semiconductor interface associated with laminated electrodes²⁹ as compared to spin coating the semiconductor film over the top of the electrodes. Additionally, the mobility of the printed devices is larger than that of the reference devices. Similar results for Pn OTFTs transfer printed onto flexible substrates were observed.^{12,23} Using x-ray diffraction and *in situ* transport measurements, the improved mobility for Pn devices was attributed to annealing under pressure of the organic thin film during the printing process.^{12,23,30} By comparison, it is reasonable to postulate that the morphology of the P3HT thin film also changes due to thermal annealing under pressure in such a way as to improve the mobility of the printed OTFT devices.

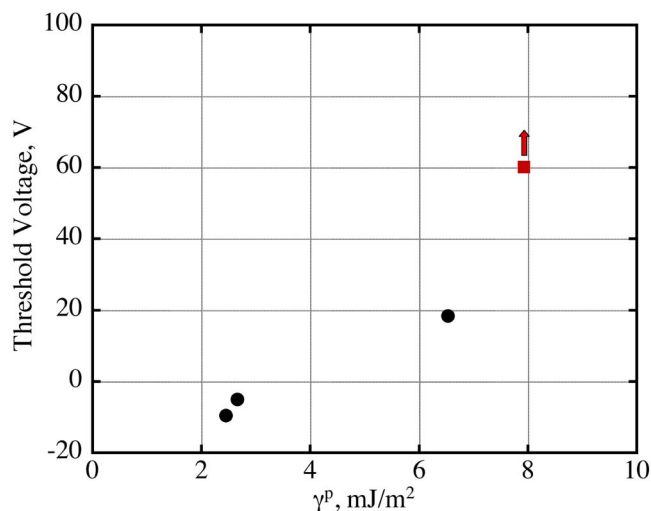


FIG. 5. (Color online) Threshold voltage vs polar component of the surface energy for P3HT devices fabricated with PMMA, PS, PC, and PHS dielectric layers. Note that the threshold voltage for the devices fabricated with PHS (red square with arrow pointing toward larger voltage) is an estimate.

Since Pn and P3HT both show improved mobility after printing, although they have very different fabrication methods and solid properties, it appears that annealing of organic thin films is a general process that, for the appropriate printing conditions, has the potential to dramatically improve the transistor properties of an organic thin film.

VI. DIELECTRIC EFFECT

The threshold voltage of an OTFT is likely to be affected by the dielectric surface, especially the presence of a surface electric dipole. Figure 5 shows the OTFT threshold voltage as a function of the polar component of the surface energy (as determined from contact angle methods³¹) of the polymer dielectric layer. The threshold voltage is seen to increase monotonically as a function of the surface energy. The addition of polar groups into a polymer structure will tend to increase the polar component of the surface energy, for example, $\gamma_p = 2.45 \text{ mJ/m}^2$ for PS as compared to $\gamma_p = 7.91 \text{ mJ/m}^2$ for poly(hydroxystyrene) (PHS). We hypothesize that these groups also increase the surface electric dipole, increasing the threshold voltage. The same polar groups also tend to increase the dielectric constant and the polarization of the bulk polymer film and hence the overall gate capacitance. Such bulk changes should have only a small effect on the threshold voltage, but more work is needed to verify the relationship between the polar surface energy and threshold voltage. Control of the threshold voltage by a care-

TABLE II. Device properties of reference and flexible P3HT OTFTs.

Device (No. of devices)	μ (cm ² /V s)	$R_c W$ (MΩ cm)	V_t (V)	On/off ratio
P3HT/SiO ₂ /Si (9) reference samples	0.007	0.56	13	$\sim 5 \times 10^4$
P3HT/PMMA/PET (15)	0.0186	0.18	18.5	$\sim 10^5$
P3HT/PS/PET (13)	0.0196	0.13	-9.5	$\sim 5 \times 10^4$
P3HT/PC/PC (14)	0.0408	0.23	-5	$\sim 10^4$

ful choice of the material properties of the dielectric layer can have importance for the design of flexible electronic circuits.

In addition to the devices listed in Table II, a set of transfer-printed P3HT OTFTs was also fabricated with PHS as the dielectric layer. These P3HT/PHS/PET devices appeared to behave as though they had a threshold voltage so large that they could not be turned off with an applied gate voltage up to +60 V. For this reason these devices have not been included in the results listed above. However, these devices are of interest in that the Pn devices with a PHS dielectric layer also exhibited a large threshold voltage in comparison to those with a PMMA dielectric layer.¹² Therefore, a data point indicating a threshold voltage in excess of 60 V (red square with arrow pointing in the direction of larger voltage) is included in Fig. 5 for a PHS dielectric layer. Clearly the semiconductor/dielectric interaction is important in terms of device performance. Others^{32,33} studied the role of dielectrics in the performance of OTFTs and showed that surface roughness, charge trapping, and surface energies are important parameters. For most of these reports, the organic semiconductor was deposited directly onto the dielectric surface. The morphology of the resulting thin film is therefore extremely sensitive to the growth process.

Transfer printing provides the advantage in that the formation of the dielectric/semiconductor interface is not a growth process but a mechanical contact between two pre-existing surfaces. Thus changes in the resulting morphology due to annealing during the transfer printing process will presumably be dependent only on differences in polymer chemistry at the semiconductor/dielectric interface.

VII. CONCLUSION

Three different polymer gate dielectrics have been used in fabricating high quality P3HT TFT devices on flexible substrates via the transfer printing process. The devices are easily assembled onto a PET substrate with either a PMMA or PS dielectric layer or onto a PC substrate with a PC dielectric layer, with minor processing changes (e.g., use of release layers) to adjust for differences in adhesion. The contact resistance of all the flexible OTFT devices presented here is notably lower than that of the unprinted reference devices. Also, the mobility of all the flexible OTFT devices presented is higher than that of the unprinted reference devices. Previous flexible devices based on Pn showed similar improvements. The threshold voltage trends monotonically with the surface energy, indicating that the choice of dielectric materials can be used to tune the properties of the resulting OTFT device. The demonstration of transfer-printed OTFTs with different substrate and dielectric materials as well as both small molecule^{11,12,30,34} and polymeric organic semiconductor materials illustrates the broad applicability of the transfer printing process.

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