VITESSE

VSC7216-01
Data Sheet

Multi-Gigabit Interconnect Chip

FEATURES

- Four ANSI X3T11 Fibre Channel and IEEE 802.3z Gigabit Ethernet-compliant transceivers
- Over 8Gb/s duplex raw data rate
- User-selectable speed modes:
  - Full-speed mode: 0.98Gb/s to 1.36Gb/s
  - Half-speed mode: 0.49Gb/s to 0.68Gb/s
- Redundant PECL Tx outputs and Rx inputs
- 8B/10B encoder/decoder per channel and optional encoder/decoder bypass operation
- ASIC-Friendly™ timing options for transmitter parallel input data
- Elastic buffers for intra-/inter-chip cable deskewing and channel-to-channel alignment
- Tx/Rx Rate matching by means of IDLE insertion/deletion
- Compatible with VSC7211, VSC7212, and VSC7214
- Received data is aligned to local reference clock or to recovered clock
- PECL Rx signal detect and cable equalization
- Per-channel serial Tx-to-Rx and parallel Rx-to-Tx internal loopback modes
- Clock multiplier generates baud rate clock
- Automatic Lock-to-Reference
- JTAG boundary scan support for TTL I/O
- Built-In Self-Test (BIST)
- 3.3V power supply
- 3.0W typical power dissipation
- 256-pin, 27mm, thermally-enhanced BGA package

APPLICATIONS

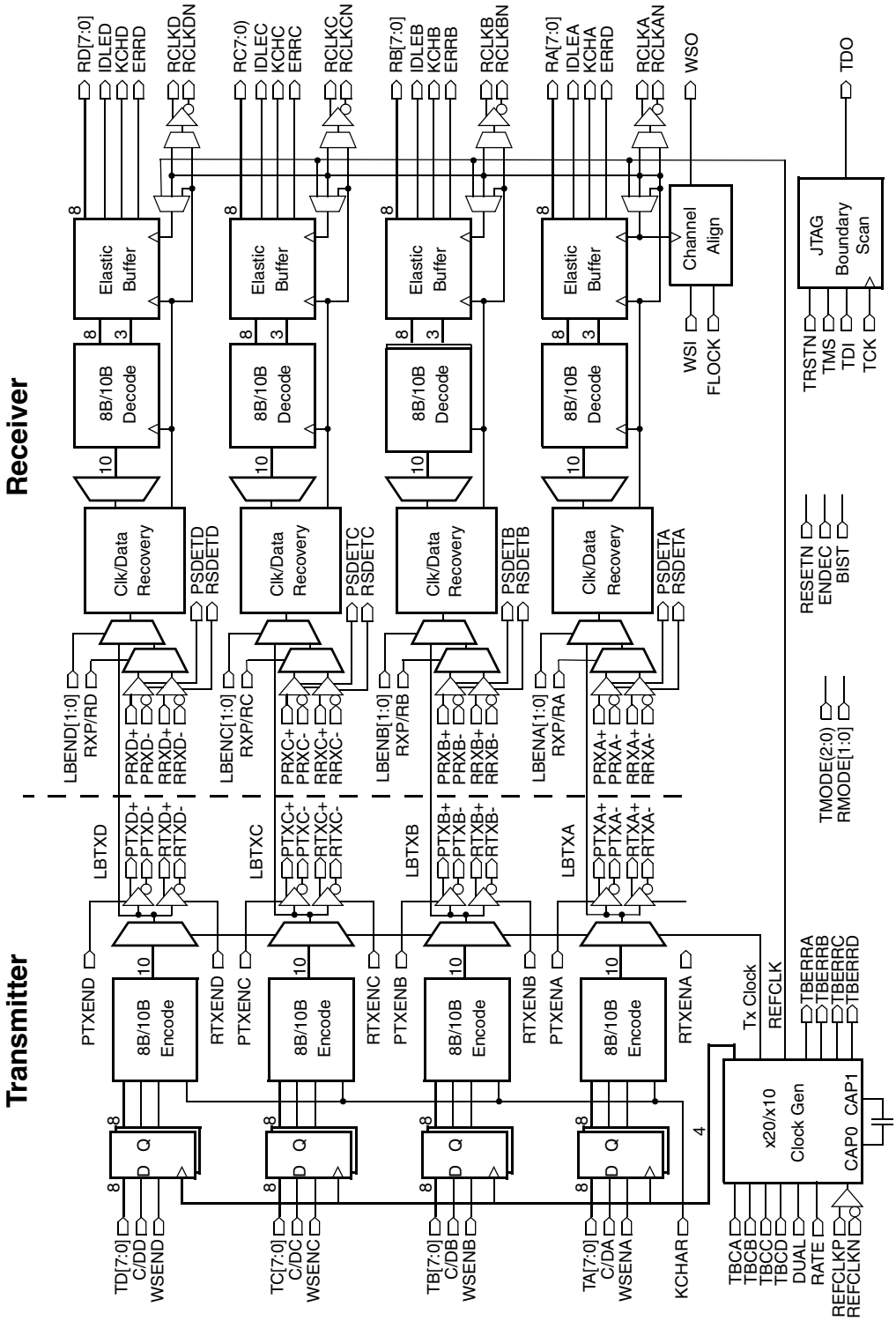
- Backplane interconnect for data communications
- Serial bus extension
- Gigabit Ethernet transceiver in 10-bit interface (TBI)
- Fibre Channel transceiver in TBI
- Serial link redundancy

GENERAL DESCRIPTION

The VSC7216-01 is a quad 8-bit parallel-to-serial and serial-to-parallel transceiver chip designed for high bandwidth interconnection between busses, backplanes, or other subsystems. Four Fibre Channel and Gigabit Ethernet-compliant transceivers provide up to 8.32Gb/s of duplex raw data transfer. Each channel is capable of operating at a data transfer rate between a maximum of 1088Mb/s (8 bits at 136MHz) or a minimum of 392Mb/s (8 bits at 49MHz). In duplex mode, the maximum aggregate transfer rate is 8.7Gb/s for the entire device. Four 8B/10B encoders, serializers/deserializers (SerDes), 8B/10B decoders, and elastic buffers provide a simple interface for transferring data serially and recovering it on the receive side. The VSC7216-01 can also be configured to operate as four non-encoded 10-bit transceivers.

The operating temperature range of the VSC7216-01 is 0°C ambient to +90°C case. For applications requiring a wider temperature range, Vitesse offers the VSC7216-03, with an extended temperature range of –40°C ambient to +95°C case.

VSC7216-01 Block Diagram



Notation

In this document, each of the four channels are identified as channel A, B, C or D. When discussing a signal on any specific channel, the signal will have the channel letter embedded in the name, for example, TA[7:0]. When referring to the common behavior of a signal that is used on each of the four channels, a lower case "n" is used in the signal name, for example, Tn[7:0]. Differential signals (for example, PTXA+ and PTXA–) may be referred to as a single signal (for example, PTXA), by dropping reference to the "+" and "–". REFCLK refers to either the PECL/TTL input pair REFCLKP/REFCLKN, which can be differential PECL (using both REFCLKP and REFCLKN), or single-ended TTL (using REFCLKP and leaving REFCLKN open).

Clock Synthesizer

Depending on the state of the DUAL input, the VSC7216-01 clock synthesizer multiplies the reference frequency provided on the REFCLK input by 10 (DUAL is LOW) or 20 (DUAL is HIGH) to achieve a baud rate clock between 0.98GHz and 1.36GHz. The on-chip phase-locked loop (PLL) uses three external 0.1µF capacitors to control the loop filter; one connected between CAP0 and CAP1 and two capacitors connected to ground. If a three-capacitor circuit cannot be used, a single differential capacitor is adequate (see C_1 in Figure 1). These capacitors should be of multilayer ceramic dielectric, or better, with at least a 5V working voltage rating and a good temperature coefficient (NPO is preferred but X7R may be acceptable). The capacitors minimize the impact of common-mode noise, especially power supply noise, on the clock multiplier unit (CMU). Higher value capacitors provide better robustness in systems. NPO is preferred because if an X7R capacitor is used, the power supply noise sensitivity will vary with temperature. Larger values are better; however, 0.1µF is adequate. These components should be isolated from noisy traces.

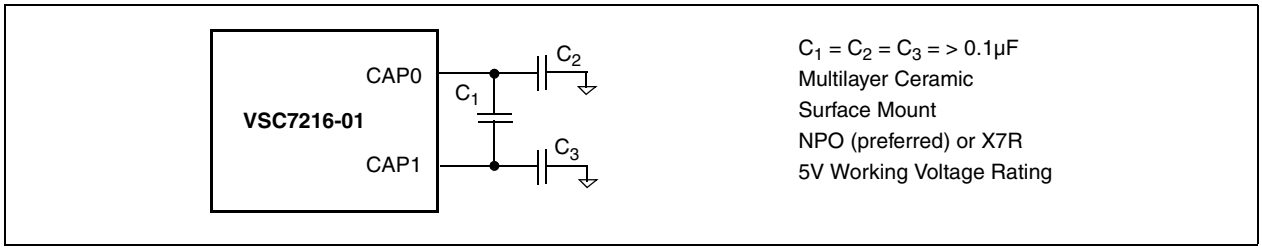


Figure 1. Loop Filter Capacitors (best circuit)

The REFCLK signal can be either single-ended TTL or differential LVPECL. If TTL, connect the TTL input to REFCLKP and leave REFCLKN open. If LVPECL, connect the inputs to REFCLKP and REFCLKN. Internal biasing resistors sets the proper DC level to $V_{DD}/2$.

Serial and parallel data rates for all channels may be halved by means of the RATE pin. When RATE is HIGH, the chip is in full-speed mode (default mode of operation), and when LOW, the half-speed mode is selected. Table 1 shows the interaction of the DUAL and RATE inputs.

Table 1. Using the RATE Input to Achieve Half-Speed Operation

RATE Pin	DUAL Pin	Clock Multiplication Factor	Serial Link Speed	Parallel Data Rate	REFCLK Frequency
0	0	x10	500Mb/s	50Mb/s	50MHz
0	1	x20	500Mb/s	50Mb/s	25MHz
1	0	x10	1Gb/s	100Mb/s	100MHz
1	1	x20	1Gb/s	100Mb/s	50MHz

Analog Power Supply Considerations

The VSC7216-01 contains an internal PLL that is powered by separate analog power supply pins, denoted as VDDA and VSSA. The performance of the VSC7216-01 is particularly sensitive to noise on these pins, therefore, special care should be taken to filter out any such noise. It is recommended that V_{DD} pass through a ferrite bead and onto the V_{DDA} pin, which should be bypassed with a pair of 0.1µF and 10µF capacitors. See Application Note AN-56, *Backplane Transceiver Design Guide,* for recommendations for these components.

TRANSMITTER FUNCTIONAL DESCRIPTION

Transmitter Data Bus

Each VSC7216-01 transmit channel has an 8-bit input transmit data character, Tn[7:0], and two control inputs, C/Dn and WSENn. The C/Dn input determines whether a normal data character or a special K-character is transmitted, and the WSENn input initiates transmission of a 16-character "Word Sync Sequence" used to align the receive channels. These data and control inputs are clocked either on the rising edge of REFCLK, on the rising edge of TBCn, or within the data eye formed by TBCn. When not using REFCLK, each channel uses either its own TBCn input or uses the TBCA input. The transmit interface mode is controlled by TMODE[2:0] as shown in Table 2.

When used, the TBCn inputs must be frequency-locked to REFCLK. No phase relationship is assumed. A small skew buffer is provided to tolerate phase drift between TBCn and REFCLK. This buffer is recentered by the RESETN input, and the total phase drift after recentering must be limited to ±180° (where 360° is one character time). Each channel has an error output, TBERRn, that is asserted HIGH to indicate that the phase drift between TBCn and REFCLK has accumulated to the point that the elastic limit of the skew buffer has been exceeded and a transmit data character has been either dropped or duplicated. This error cannot occur when input timing is referenced to REFCLK. The TBERRn output timing is identical to the low-speed receiver outputs, as selected by RMODE[1:0] in Table 6.

Table 2. Transmit Interface Input Timing Mode

TMODE[2:0]	Input Timing Reference
0 0 0	REFCLK rising edge
0 0 1 0 1 0 0 1 1	Reserved
1 0 0	TBCA rising edge
1 0 1	TBCn rising edge
1 1 0	TBCA data eye
1 1 1	TBCn data eye

Figures 2, 3, and 4 show possible relationships between data and control inputs and the selected input timing source. Figure 2 shows how REFCLK is used as an input timing reference. This mode of operation is used in the VSC7211 and VSC7214. Figure 3 and Figure 4 show how TBCn is used as an input timing reference. When TBCn is used to define a data eye, as shown in Figure 4, it functions as an additional data input that simply toggles every cycle.

The REFCLK and TBCn inputs are not used directly to clock the input data. Instead, an internal PLL generates edges aligned with the appropriate clock. The arrows on the rising edges of these signals define the reference edge for the internal phase detection logic. An internal clock is generated at $1/10^{th}$ the serial transmit data rate that is locked to the selected input timing source. This is especially important when DUAL is HIGH and input timing is referenced to REFCLK since the falling edge is *not* used. In this mode, the internal clock's rising edges are placed coincident with REFCLK's rising edges, halfway between REFCLK's succeeding rising edges.

A similar situation exists when TBCn is used to define a data eye; only the rising edges of TBCn are used to define the external data timing. The internal clock active edges are placed at 90° and 270° points between consecutive TBCn rising edges (which are assumed to be 360° apart).

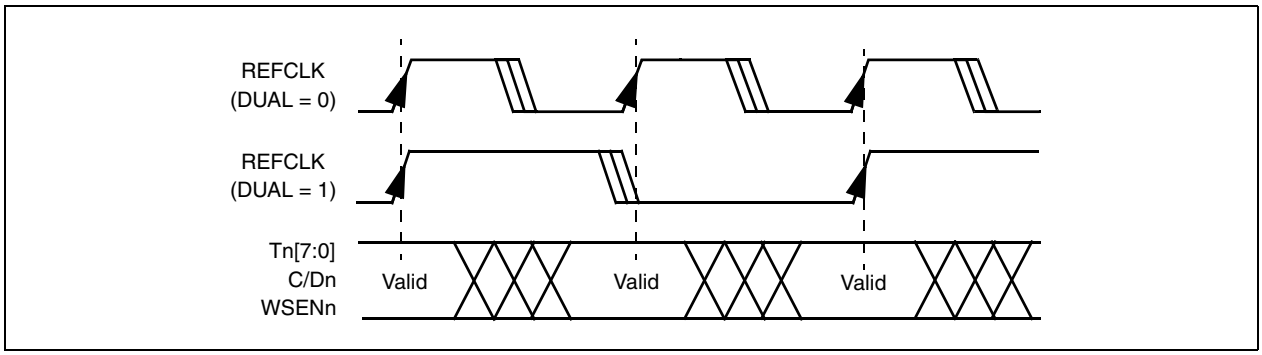


Figure 2. Transmit Timing, TMODE[2:0] = 000

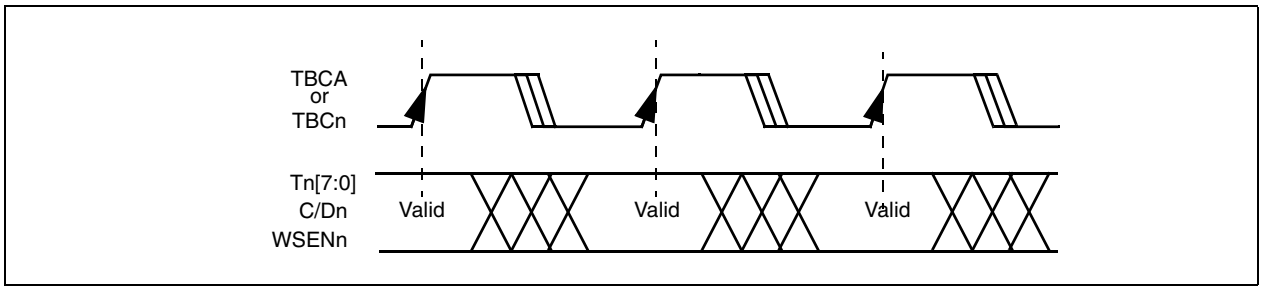


Figure 3. Transmit Timing, TMODE[2:0] = 10x

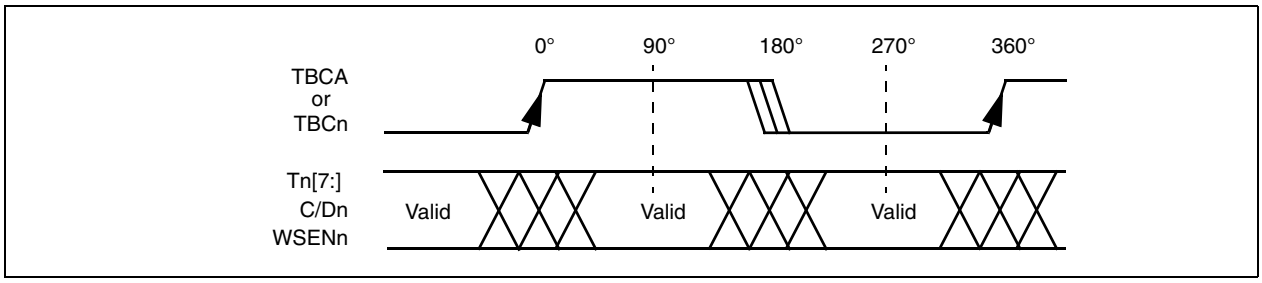


Figure 4. Transmit Timing, TMODE[2:0] = 11x (ASIC-Friendly TIming)

8B/10B Encoder

Each channel contains an 8B/10B encoder that translates the 8-bit input data on Tn[7:0] into a 10-bit encoded data character. Each channel also incorporates C/Dn inputs which, along with KCHAR, allow the transmission of special Fibre Channel Kxx.x characters (see Table 3). Note that KCHAR is a static input, and *does not* have the same input timing as Tn[7:0], C/Dn, and WSENn. Normally C/Dn is LOW in order to transmit data. If C/Dn is HIGH and KCHAR is LOW, then a Fibre Channel defined IDLE character (K28.5 = 0011111010 or 1100000101, depending on disparity) is transmitted and Tn[7:0] is ignored. If C/Dn is HIGH and KCHAR is HIGH, a Kxx.x character is transmitted as determined by the data pattern on Tn[7:0] (see Table 4). Data patterns other than those defined in Table 4 produce undefined 10B encodings.

Table 3. Transmit Data Controls

WSENn	C/Dn	KCHAR	Encoded 10-Bit Output
0	0	X	Data character
0	1	0	IDLE character (K28.5)
0	1	1	Special Kxx.x character
1	X	X	16-character Word Sync Sequence

Table 4. Special Characters (selected when C/Dn and KCHAR are HIGH)

Code	Tn[7:0]	Comment	Code	Tn[7:0]	Comment
K28.0	000 11100	User-defined	K28.5-	101 01101	User-defined
K28.1	001 11100	User-defined	K28.6	110 11100	User-defined
K28.2	010 11100	User-defined	K28.7	111 11100	Test only
K28.3	011 11100	User-defined	K23.7	111 10111	User-defined
K28.4	100 11100	User-defined	K27.7	111 11011	User-defined
K28.5	101 11100	IDLE	K29.7	111 11101	User-defined
K28.5+	101 01100	User-defined	K30.7	111 11110	User-defined

Encoder Bypass Mode

When ENDEC is LOW, the 8B/10B encoders are bypassed, and a 10-bit input character Tn[7:0] is serialized directly in each channel; bit Tn0 is transmitted first. The C/Dn input becomes Tn8, and WSENn becomes Tn9. The KCHAR input becomes ENCDET, which is not used in the transmitter, but when HIGH, enables “comma” detection in all four receivers. For a description of this mode of operation in the receiver, see “Decoder Bypass Mode” on page 15. The latency through the transmitter is reduced by one character time when ENDEC is LOW. This mode of operation is similar to a 10-bit interface commonly found in serializer/deserializers for Fibre Channel and Gigabit Ethernet markets.

Word Sync Generation

The VSC7216-01 performs channel alignment (also referred to as “word alignment” or “word sync”), which means that the four receive data output streams are aligned in such a way that the same 4-byte word presented to the four transmit channel inputs for serialization are transferred on the receive channel parallel outputs. The Word Sync Sequence provides a unique synchronization point in the serial data stream that is used to align the receive channels. This sequence consists of 16 consecutive K28.5 IDLE characters, with disparity reversals on the second and fourth characters. The Word Sync Sequence is sent either as:

- I+ I+ I- I- I+ I- I+ I- I+ I- I+ I- I+ I- I+ I-, or
- I- I- I+ I+ I- I+ I- I+ I- I+ I- I+ I- I+ I- I+

The Word Sync Sequence that is sent depends on the transmitter’s running disparity at the time the first IDLE character is serialized.

Transmission of the Word Sync Sequence is initiated independently in each channel when the WSENn input is asserted HIGH for one character time (see Figure 5). When WSENn is HIGH, the C/Dn and Tn[7:0] inputs are ignored. The WSENn, C/Dn, and Tn[7:0] inputs are also ignored for the subsequent 15 character times. The Word Sync Sequence, shown in Figure 5, is initiated in cycle W1 and transmitted through cycle W16. Normal data transmission (or the transmission of another Word Sync Sequence) resumes in cycle D3. Figure 5 is illustrated with the assumption that input timing is referenced to REFCLK (for example, TMODE[2:0] = 000) with the DUAL input LOW. As long as WSENn remains asserted, another Word Sync Sequence is generated.

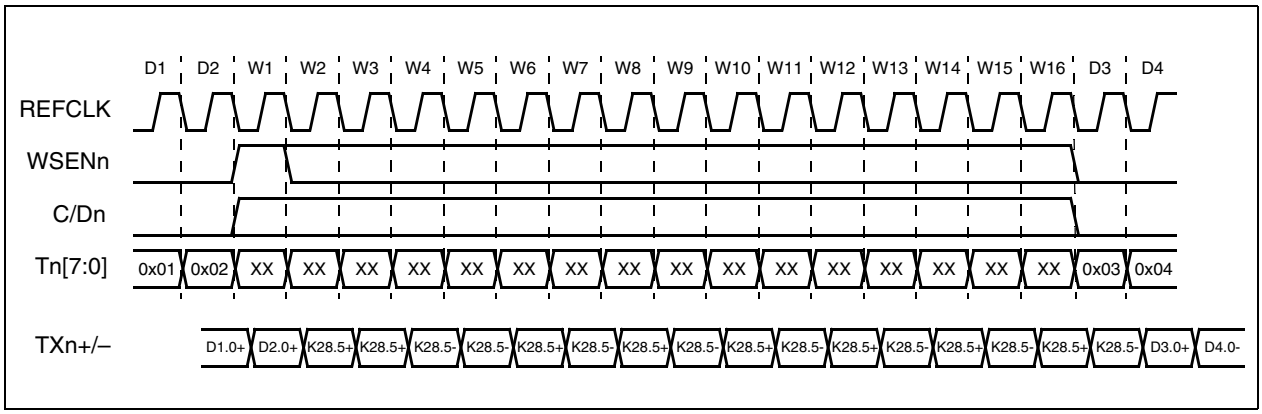


Figure 5. Word Sync Sequence Generation

Serializer

The 10-bit output from the encoder (or from the encoder input register if ENDEC is LOW) is fed into a multiplexer, which serializes the parallel data using the synthesized transmit clock. The least significant bit (LSB) of the 10B data is transmitted first. Each channel has both primary and redundant serial output ports. The primary port is labeled PTXn and the redundant port is labeled RTXn. The ports consist of differential PECL output buffers that operate either 10 or 20 times the REFCLK rate. The primary and redundant transmitter outputs are separately controlled on each channel. The primary PECL outputs (PTXn) are enabled when the PTXENn input is HIGH, and the redundant

PECL outputs (RTXn) are enabled when the RTXENn input is HIGH. When a PECL output is disabled, the associated output buffers do not consume power, and the attached pins are undriven. Performance of the PECL outputs is optimized when terminated as shown in Figure 6.

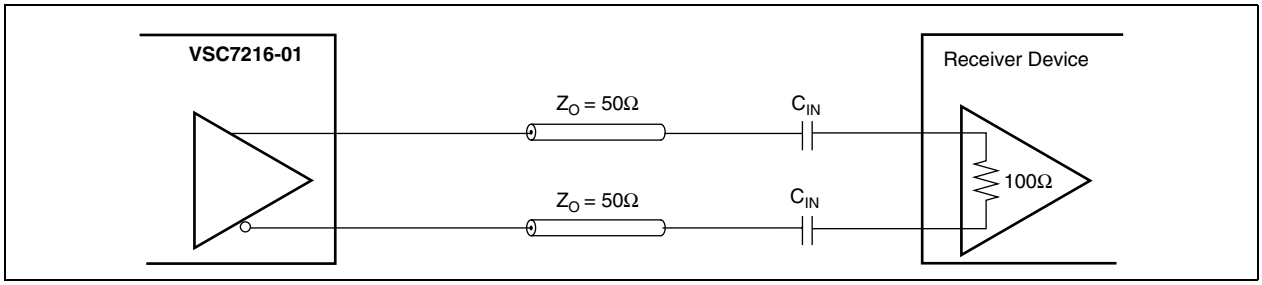


Figure 6. Recommended PECL Output Termination Scheme

If using the VSC7216-01 as a replacement for the VSC7216, the termination scheme in Figure 7 can be used. The outputs will function normally, but with slightly increased jitter and power consumption.

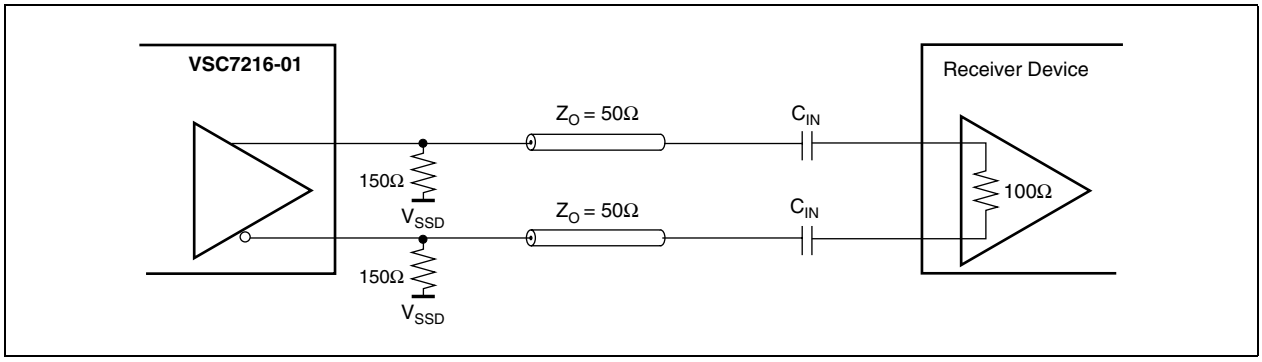


Figure 7. PECL Output Termination Scheme With Pull-Downs

Receiver Functional Description

Serial Data Source

Each receive channel has both primary and redundant serial input ports. The primary port is labeled PRXn and the redundant port is labeled RRXn. The ports consist of differential PECL input buffers. Each channel also has a control input, RXP/Rn, that selects either the primary or redundant serial input as the data source for that channel. For example, when RXP/RC is HIGH, Channel C's serial data source is PRXC. When LBENn[1:0] = 10, the channel's transmitter is looped back and becomes the serial data source, regardless of the state of RXP/Rn (see Table 5).

Table 5. Serial Data Source Selection

LBENn[1:0]	RXP/Rn	Serial Data Source
≠ 1 0	0	RRXn
≠ 1 0	1	PRXn
= 1 0	X	LBTXn Loopback from transmitter

Signal Detection

Each channel's primary and redundant PECL input buffers have an associated signal detect output: PSDETn and RSDETn. All eight outputs are available for continuous monitoring of both the selected and non-selected input. Each signal detect output is asserted HIGH when transitions are detected on the associated PECL input and the signal amplitude exceeds 200mV. A LOW indicates that either no transitions are detected or the signal amplitude is below 80mV. The signal detect outputs are considered undefined when the signal amplitude is in the 80mV to 200mV range. The signal detect circuitry behaves like a retriggerable one-shot that is triggered by signal transitions and whose time-out interval ranges from 40 to 80 bit times. The transition density is not checked to ensure that it corresponds to a valid Fibre Channel data stream. The PSDETn and RSDETn output timing is identical to the low-speed receiver outputs, as selected by RMODE[1:0] in Table 6.

Receiver Equalization

Typically, incoming data on the PRX/RRX inputs contains a substantial amount of Inter Symbol Interference (ISI) or deterministic jitter, which reduces the ability of the receiver to recover data without errors. An equalizer in the receiver's input buffers compensates for this deterministic jitter. This circuit has been designed to effectively reduce the ISI commonly found in copper cables or backplane traces due to low frequencies traveling faster than high frequencies as a result of the skin effect. The equalizer boosts high frequency edge response to reduce the adverse effects of ISI.

Clock and Data Recovery

At the receiver, each channel contains an independent clock recovery unit (CRU) that accepts the selected serial input source, extracts the high-speed clock, and retimes the data. Each CRU automatically locks onto data, and if data is not present, the CRU automatically locks onto the reference clock, which maintains a very well-behaved recovered clock (RCLKn/RCLKNn) that does not contain any slivers. The recovered clock operates at a frequency of the REFCLK reference, ±200ppm. The use of an external Lock-to-Reference pin is not required.

The CRU must perform bit synchronization that occurs when the CRU locks onto and properly samples the incoming serial data, as described in the previous paragraph. When the CRU is not locked onto the serial data, the 10-bit data out of the decoder is invalid, which results in numerous 8B/10B decoding errors or disparity errors. When the link is disturbed (for example, the cable is disconnected or the serial data source is switched), the CRU will require a certain amount of time to lock onto data, which is defined in the Data Acquisition Lock Time parameter in Table 15.

Deserializer and Character Alignment

The retimed serial data stream is converted into 10-bit characters by the deserializer. A special 7-bit comma pattern, 0011111xxx or 1100000xxx, is recognized by the receiver and allows it to identify the 10-bit character boundary. This pattern is found in three special characters: K28.1, K28.5, and K28.7. However, K28.5 is chosen as the unique IDLE character. Only K28.1 and K28.5 characters should be used in normal operation. The K28.7 character should be reserved for test and characterization use.

Character alignment occurs when the deserializer synchronizes the 10-bit character framing boundary to a comma pattern in the incoming serial data stream. If the receiver identifies a comma pattern in the incoming data stream that is misaligned to the current framing boundary, the receiver will resynchronize the recovered data to align the data to the new comma pattern. Resynchronization ensures that the comma character is output on the internal 10-bit bus so that bits 0 through 9 equal 0011111xxx or 1100000xxx. If the comma pattern is aligned with the current framing boundary, resynchronization will not change the current alignment. Resynchronization is always enabled and cannot be turned off when ENDEC is HIGH. After character resynchronization, the VSC7216-01 ensures that within a link, the 8-bit data sent to the transmitting VSC7216-01 will be recovered by the receiving VSC7216-01 in the same bit locations as the transmitter (for example, Tn[7:0] = Rn[7:0]). When ENDEC is LOW, comma detection, and alignment are enabled only if KCHAR is HIGH.

10B/8B Decoder

The 10-bit character from the deserializer is decoded in the 10B/8B decoder, which outputs the 8B data byte and three bits of status information. If the 10-bit character does not match any valid value, an out-of-band error is generated, which is output on the receiver status bus. Similarly, if the running disparity of the character does not match the expected value, a disparity error is generated. The decoder also reports when a K-character is received and distinguishes the K28.5 (IDLE) character from other K-characters. This status information is combined with LOS State Machine status and FIFO error status to produce the prioritized per-character link status output information (see Table 8 on page 17).

Elastic Buffer and Channel Deskewing

Elastic buffers are included in each of the four receive channels. Decoded data and status information is written into these buffers on each channel's recovered clock and is read on the selected output clock. In addition to allowing decoded data to easily cross from a channel's recovered clock domain to its output clock domain, the elastic buffers facilitate two other functions. Through inter-channel deskewing, they allow channel alignment (the reconstruction of a multi-byte word as presented to the transmitting devices). They also facilitate rate matching through IDLE character insertion/deletion when the channel's recovered clock is not frequency-locked to its output clock.

There are three conditions under which a receive channel's elastic buffer is recentered. The RESETN input, when asserted, recenters the read/write pointers in each elasticity buffer. Whenever a comma character is received that changes the receive character's framing boundary, the elasticity buffer is recentered. Lastly, it is also recentered

whenever the receiver detects the synchronization point in the Word Sync Sequence. All three of these events are associated with chip initialization or link initialization and would not occur during normal data transfer. Note that recentering can result in the loss or duplication of decoded character data and status information.

When a condition changes transmit timing (for example, phase shifts in TBC) or shifts phase/alignment into the receiver, a Word Sync Event should be initiated to recenter all elasticity buffers. Otherwise, data corruption could occur.

The VSC7216-01 presents recovered data on Rn[7:0] and status on IDLEn, KCHn, and ERRn. These outputs are timed either to each channel's own recovered clock (RCLKn/RCLKNn), to Channel A's recovered clock (RCLKA/RCLKNA), or to REFCLK. The output timing reference is selected by RMODE[1:0] (see Table 6). The transmitter input skew buffer error outputs TBERRn, and the analog signal detect outputs (PSDETn and RSDETn) are also synchronized to the selected output timing reference. There are two choices for REFCLK-based timing that differ in the positioning of the data valid window associated with the output signals timed to REFCLK: when RMODE[1:0] = 00, REFCLK is approximately centered in the output data valid window as in the VSC7214 and when RMODE[1:0] = 01, REFCLK slightly leads the data valid window so that output data appears to have a more typical "clock-to-Q" timing relationship to REFCLK.

Table 6. Receiver Interface Output Timing Mode

RMODE[1:0]	Output Timing Reference
0 0	REFCLK (centered)
0 1	REFCLK (leading)
1 0	RCLKA/RCLKNA
1 1	RCLKn/RCLKNn

The term "word clock" is used for whichever clock—REFCLK, RCLKA/RCLKNA, or RCLKn/RCLKNn—is selected as the output timing reference. If RMODE[1] is HIGH, each channels' RCLKn/RCLKNn outputs are complementary outputs at $1/10^{th}$ or $1/20^{th}$ the baud rate of the incoming data, depending upon DUAL. When RCLKA/RCLKNA is selected as the output timing reference, the RCLKn/RCLKNn outputs of Channel B, C, and D are copies of RCLKA/RCLKNA. If RMODE[1] is LOW, then each channels' RCLKn/RCLKNn outputs are held in a LOW/HIGH state, respectively, and the data and status outputs are timed to REFCLK. If DUAL is HIGH, all data at the four output ports are synchronously clocked out on both positive and negative edges of the selected word clock at $1/20^{th}$ the baud rate. If DUAL is LOW, the data is clocked out of the VSC7216-01 only on the rising edge of the selected word clock at $1/10^{th}$ the baud rate. Figure 8, Figure 9, and Figure 10 show the output data and status timing waveforms.

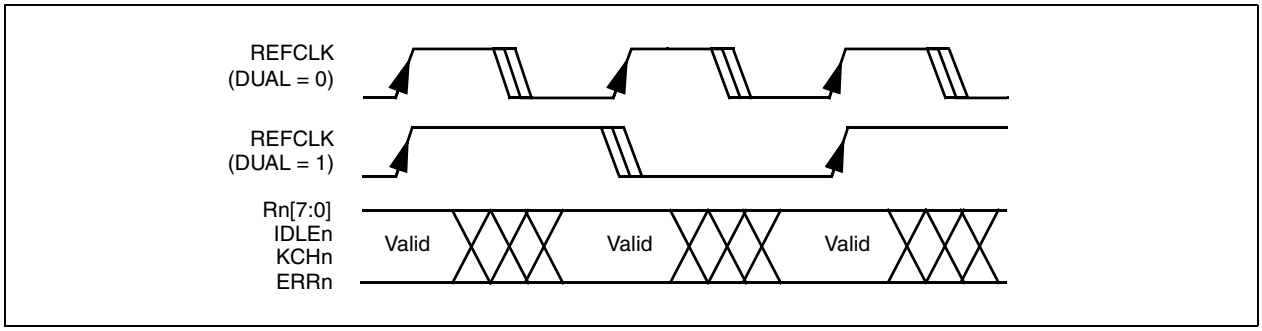


Figure 8. Receive Timing, RMODE[1:0] = 00

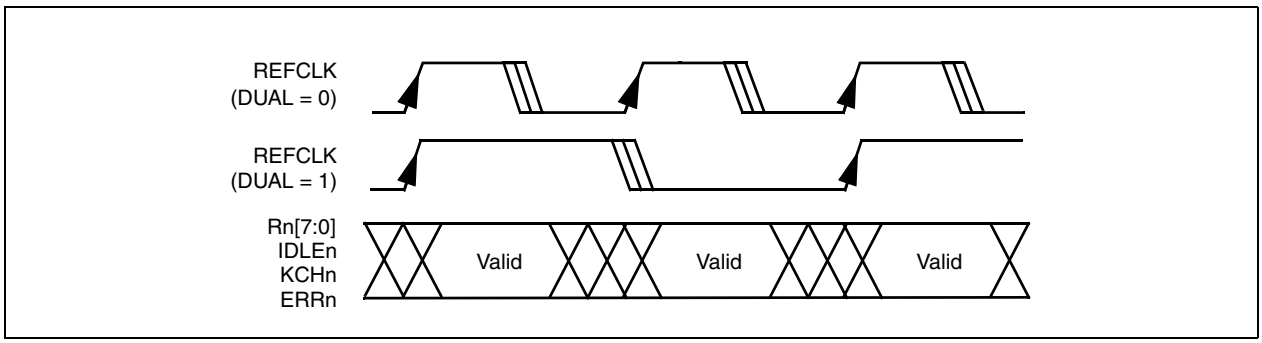


Figure 9. Receive Timing, RMODE [1:0] = 01

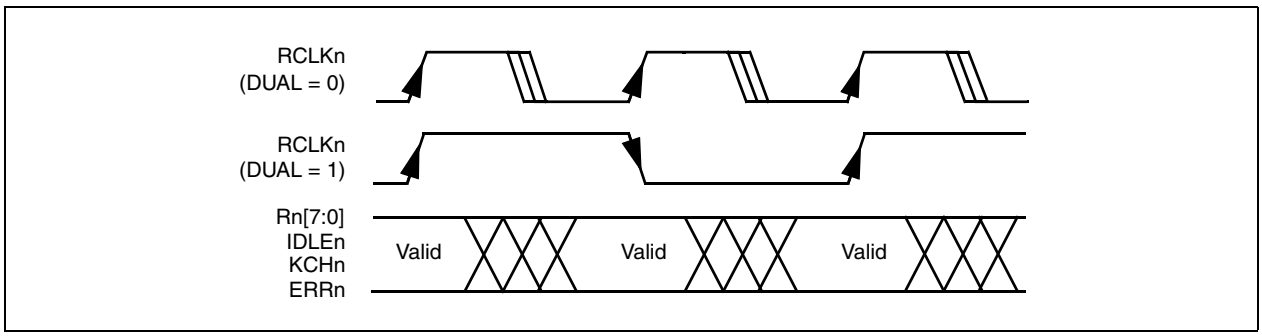


Figure 10. Receive Timing, RMODE[1:0] = 1x

The data coming from the decoder is clocked into the elastic buffer by the recovered clock from the channel's CRU. The data is clocked out of the elastic buffers with a word clock. If the transmitting device's REFCLK is not precisely frequency-locked to a receive channel's word clock, the channel's elastic buffer will gradually fill or empty as the recovered clock (which is by definition frequency-locked to the transmitter's REFCLK) steadily drifts in phase relative to the word clock.

To accommodate frequency differences between a transmitter's REFCLK and the word clock, the VSC7216-01 automatically performs rate matching by either deleting or duplicating IDLE characters. The FLOCK input must be LOW to enable rate matching which, based on how the WSI input is connected, performs either in each channel individually or in parallel across a group of channels that are word-aligned. See "Word Alignment" on page 13 for more information. It is the user's responsibility to ensure that the frequency at which IDLEs are simultaneously transmitted on each channel accommodates the frequency differences, if any, in their system architecture. Underrun/overrun errors could result if the IDLE density requirements are not met. The use of a continuous stream of IDLE characters should be avoided when rate matching is enabled. The IDLE addition/deletion logic relies on the status bits to identify K28.5 IDLE characters (see Table 8). The use of continuous IDLE characters forces the VSC7216-01 into the RESYNC state (see Figure 11), which results in a status bit sequence that the addition/deletion logic does not recognize as an IDLE character.

The elastic buffer is designed to allow a maximum phase drift of ±2 serial clock bit times between resynchronizations, which sets a limit on the maximum data "packet" length allowed between IDLEs. This maximum packet length depends on the frequency difference between the transmitting and receiving device's REFCLKs.

Let $\Delta\phi$ represent phase drift in bit times, and let 2π represent one full 10-bit character of phase drift. Limiting phase drift to two bit times means the following inequality must be satisfied:

$$\Delta\phi \leq ((0.2) \times 2\pi) \quad \textbf{(EQ 1)}$$

Let L be the number of 10-bit characters transmitted, and let Δf be the frequency offset in ppm. The total phase drift in bit times is given by:

$$\Delta\phi = (\Delta f / 10^6) \times 2\pi L \quad \textbf{(EQ 2)}$$

A simple expression for maximum packet length as a function of frequency offset is derived by substituting (EQ 2) in (EQ1) and solving for L:

$$L \leq (0.2 \times 10^6) / \Delta f \quad \textbf{(EQ 3)}$$

As an example, if the frequency offset is 200ppm, then the maximum packet length should not be more than 1K bytes. To increase the maximum packet length, L, decrease the frequency offset, Δf. Note that if only one K28.5 character is transmitted between "packets" of data, it may be dropped during compensation for phase drift. If the user must have at least one K28.5 character between these two packets, then two K28.5 characters must be transmitted.

Word Alignment

The VSC7216-01 performs channel-to-channel word alignment. In this mode of operation, if the data from all four channels on the transmitting VSC7216-01 (for example, the four Tn[7:0] busses) is viewed as a 32-bit word, the receiving VSC7216-01 recovers an identical word. In other words, if a transmit pattern is "ABCD", "EFGH", "IJKL", and so on, the receiver will not recover data words as "ABGD", "EFKH", "IJOL", and so on. This word alignment requires that the four transmit channels obtain input data on a common clock (for example, TMODE[2:0] = 000 or 1X0), and that the four receive channels present output data on a common word clock (for example, RMODE[1:0] = 0X or 10).

Elastic buffers within the receiver are used to deskew the four channels and align them to a common word clock. An elastic buffer allows the channels' input to be skewed up a selectable number of bit times to accommodate circuit imperfections or differences in transmission delay and jitter. Three levels of deskewing are possible, and the desired level is set with the RXFIFO0 and RXFIFO1 pins. The receiver latency and the ability to perform chip-to-chip word alignment are also affected by these settings. These relationships are shown in Table 7.

In order to perform word alignment, a synchronization point must be seen across all aligned receive channels within a ±6-bit time window. The VSC7216-01 receiver recognizes the first four characters of the Word Sync Sequence (either K28.5+ K28.5+ K28.5– K28.5– or K28.5– K28.5– K28.5+ K28.5+) as the synchronization point. As a model for understanding, consider the case where a VSC7216-01 transmitter sends 32 bits of data to the receiver through copper media, which has small cable length differences causing a channel-to-channel skew: All transmit channels that are to be word aligned transmit the Word Sync Sequence in parallel. On detection of the synchronization point, the receivers reposition the recovered data within their elastic buffers in order to align all channels and remove any channel-to-channel skew. All normal data characters following the Word Sync Sequence are properly word aligned. In the

process of channel alignment, one or two of the final twelve K28.5 characters in the Word Sync Sequence may be deleted or duplicated. This process ensures that each transmitted 32-bit word is recovered correctly.

The VSC7216-01 performs rate matching in word-aligned applications by inserting or deleting IDLEs in parallel across the aligned receive channels. This type of rate matching requires that the word-aligned data streams contain IDLEs inserted in parallel on all transmit channels (for example, an IDLE “word”) in accordance with the IDLE density requirement previously described.

Word alignment is enabled by connecting the WSI input to a WSO output, either from the same device if a single device is used or from another device if multiple devices are used in parallel to align more than four channels. The FLOCK input state and WSI input source determines whether or not rate matching (IDLE deletion or duplication) will be performed, and whether it is done independently on each channel or in parallel across aligned channels. Word alignment is disabled when WSI is not connected to a WSO output. Rate matching is disabled when either FLOCK is HIGH or WSI is held LOW (see Table 7).

Table 7. Word Alignment and Rate Matching Control

FLOCK	WSI Source	Word Alignment	Rate Matching
0	0	Off	Off
0	1	Off	Enabled, independent channels
0	WSO	Enabled	Enabled, aligned channels
1	0	Off	Off
1	1	Off	Off
1	WSO	Enabled	Off

There are four distinct modes of operation, which are defined in Table 7. The first row disables both word alignment and rate matching. (The fourth and fifth row configurations function identically to the first row.) The second row configures the channels to operate independently with rate matching. Word alignment is disabled, and IDLEs are independently dropped/duplicated in each channel as required. The third row configures the device to perform word alignment and rate matching. The receive channels are aligned per the device driving WSO, and IDLE words are dropped/duplicated across the aligned channels as required. The last row configures the device to perform both word alignment and to disable rate matching. This mode of operation is appropriate for a frequency-locked application where it’s desired to align the receive channels without altering the received data streams.

Using Multiple VSC7216-01s in Parallel

Multiple VSC7216-01s can be used in parallel to form wider bus widths. For word alignment to function correctly across multiple devices, each transmit channel’s input data must be transmitted on a common clock, and each receive channel’s output data must also be aligned to a common word clock. This alignment requires that all transmitting devices use either the same or identical REFCLKs. The alignment also requires that TMODE[2:0] = 000 (for inputs timed to REFCLK) or TMODE[2:0] = 1X0 (for inputs timed to TBCA). If inputs are timed to TBCA, then all transmitting devices must use either the same or identical TBCAs. Because all receive channels must use a common word clock, the receiving devices must also use the same or identical REFCLKs, and it must be selected as the word clock for all receive channels (RMODE[1:0] = 0X).

If the transmitting devices' REFCLKs are not frequency-locked to the receiving devices' REFCLKs, IDLEs will have to be added to or dropped from all the channels at the same time. In order to implement this, one VSC7216-01 is arbitrarily chosen as the "master" and its WSO output is driven to the WSI inputs of all the receiving VSC7216-01s, including itself. WSO is asserted prior to the VSC7216-01 adding/dropping IDLEs so all the VSC7216-01s will operate simultaneously. WSO uses a simple 3-bit serial protocol, synchronous to the master channel's word clock, for indicating the required synchronization action to other VSC7216-01s. A steady LOW level indicates no action is required. A "101" indicates that Master Channel A has seen a word sync event. The relative timing relationship between receiving a word sync event (on all channels together) and seeing 101 on the WSI input in the other channels allows these channels to word-synchronize with Master Channel A. A "110" indicates that the next IDLE encountered in the receive data stream should be deleted. A "111" indicates that an IDLE should be inserted after the next IDLE encountered in the receive data stream. Note that the arbitrarily chosen Master Channel A must be an active channel.

Decoder Bypass Mode

If ENDEC is LOW, the 8B/10B decoder is bypassed and a 10-bit received character Rn[9:0] is output from each receive channel. The KCHn output becomes Rn8, and ERRn becomes Rn9. Character alignment is handled differently in this mode of operation. As mentioned in "Encoder Bypass Mode" on page 6, the KCHAR input becomes ENCDET, which enables comma detection and resynchronization when HIGH, and disables resynchronization when LOW. Only the 0011111xxx version of the comma pattern is recognized when ENDEC is LOW. The IDLEn output becomes COMDET (comma detect), which signals detection of the 0011111xxx comma pattern in the current 10-bit output character when HIGH. This mode of operation is equivalent to a 10-bit interface commonly found in serializer/deserializers for the Fibre Channel and Gigabit Ethernet markets.

To compensate for REFCLK variations between transmitting and receiving devices, the logic used to align the four receive channels and/or insert and delete IDLE characters is disabled when ENDEC is LOW. For this mode of operation to function without errors, the word clock source, as selected by RMODE[1:0], must be frequency-locked to the REFCLK of the remote transmitting device in each channel. This is assured when RMODE[1:0] = 11. For other choices of RMODE[1:0], the frequency-locked condition must be ensured by system design. When DUAL is HIGH and RMODE[1:0] = 10 or 11, the character containing the 0011111xxx comma pattern is aligned to RCLKn/RCLKNn in each channel so that COMDET is asserted on the falling edge of RCLKn (rising edge of RCLKNn). This is done by adjusting the latency through the elastic buffer; the recovered clock is never stretched or slivered. If the comma pattern changes the framing boundary, data characters prior to the assertion of COMDET on the falling edge of RCLKn may be corrupted.

Receiver State Machine

Each channel contains a Loss of Synchronization State Machine (LSSM), which is responsible for detecting and handling loss of bit, channel, word, and word clock synchronization in a controlled manner. The three states in the LSSM: LOSS_OF_SYNC, RESYNC, and SYNC_ACQUIRED, are shown in the state diagram of Figure 11. The RESYNC state is entered when a 10-bit word has been received that contains the 7-bit comma pattern (for example. a K28.5 IDLE character). After entering the RESYNC state, the VSC7216-01 remains in the state until a valid, non-comma transmission is received. The VSC7216-01 then transitions to the SYNC_ACQUIRED state, indicating a normal operating condition. The RESYNC state is re-entered if four consecutive commas are received or if a single comma is received that changes the 10B character framing boundary. The LOSS_OF_SYNC state is entered whenever four consecutive invalid transmissions have been detected or when the occurrences of invalid transmission outnumber those of valid transmission by four. The relative occurrences of invalid vs. valid transmissions are

monitored with a simple up/down counter that increments when an invalid transmission is detected and decrements otherwise. The LSSM transitions to the LOSS_OF_SYNC state when the counter reaches four, and the counter is reset. Figure 12 shows a state diagram for the invalid transmission counter. The VSC7216-01 receiver remains in the LOSS_OF_SYNC state until a valid comma pattern is detected. Note that the RESYNC state is entered whenever the 10B framing boundary is changed, and whenever the Word Sync Sequence is received. When ENDEC is LOW, the ERRn, KCHn, and IDLEn outputs are redefined, and the decoder and associated LSSM logic in each channel is unused.

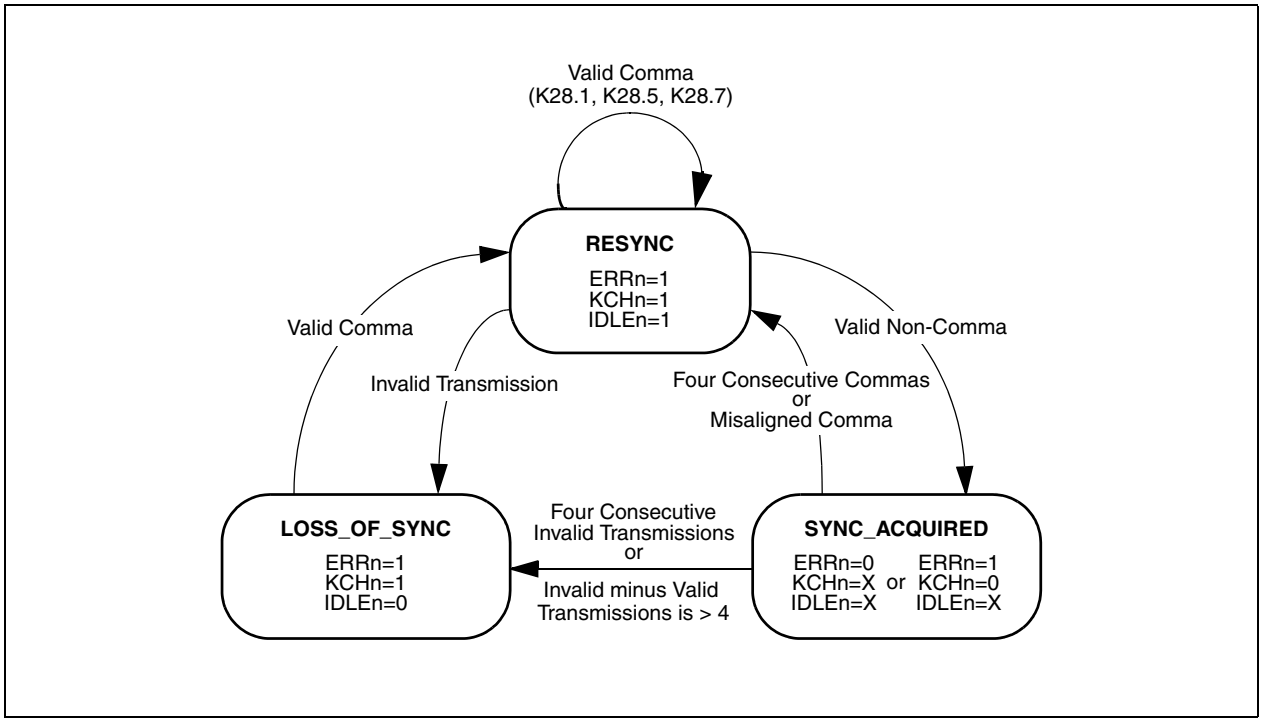


Figure 11. State Diagram of the Loss of Synchronization State Machine

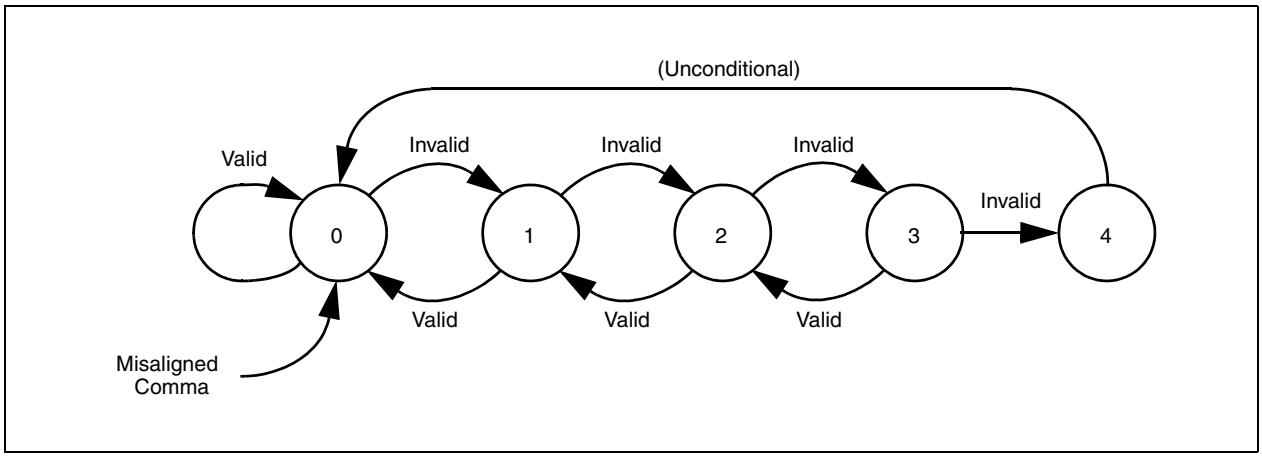


Figure 12. State Diagram of the Invalid Transmission Counter

Link Status Outputs

The ERRn, KCHn, and IDLEn outputs of the receiver indicate the status for each channel as shown in Table 8. This status is encoded, and because multiple conditions could occur simultaneously, the states are prioritized as indicated in Figure 8, with 1 being highest priority. For example, if both out-of-band and disparity errors occur, only an out-of-band error is reported because it has higher priority.

The ERRn, KCHn and IDLEn status signals apply to the data on Rn[7:0] on a per-character basis. The only exception to this is the underrun/overrun indication, which is asserted coincident with the duplicated character when an underrun occurs and is asserted following the deleted character (for example, on the cycle where the deleted character should have appeared when overrun occurs).

Table 8. Receiver Status Signals

ERRn	KCHn	IDLEn	Priority	Link Status
0	0	0	7	Valid Data Transmission: A valid 10B data character with correct disparity was received. The correctly decoded version of this character is on Rn[7:0].
0	0	1	1	Underrun/Overrun Error: The elastic buffer has not been able to add/drop an IDLE when required. Data on Rn[7:0] is invalid.
0	1	0	6	Kxx.x Special Character Detected (not IDLE): A valid 10B special character with correct disparity was received. The correctly decoded version of this character, per Table , is on Rn[7:0].
0	1	1	5	IDLE Detected: A valid IDLE character (K28.5) with correct disparity was received. The correctly decoded version of this character is on Rn[7:0]. See Table 4.
1	0	0	3	Out-of-Band Error Detected: A character was received that was not a valid 10B data or control character. Data on Rn[7:0] is invalid.
1	0	1	4	Disparity Error Detected: A valid 10B character was received that did not have the expected disparity. Rn[7:0] is invalid.
1	1	0	2	Loss of Synchronization: The receiver state machine is in the Loss-of-Sync state. Data on Rn[7:0] is invalid.
1	1	1	2	RESYNC: The receiver state machine is in the Resynchronization state. Data on Rn[7:0] is a decoded version of K28.1, K28.5, or K28.7.

Loopback Operation

Loopback control pins, LBENn[1:0], are provided in each channel to internally loop back data paths for on-chip diagnosis. Both serial and parallel loopback functions are provided.

Table 9. Loopback Mode Selection

LBENn[1:0]	Loopback Mode
0 0	Normal operation
0 1	Internal parallel loopback
1 0	Internal serial loopback
1 1	Reserved

When LBENn[1:0] = 10, Serial Loopback mode is selected. The transmitter's serial transmit data is internally connected to the receiver's CRU input. The serial loopback paths are labeled LBTXn in the VSC7216-01 block diagram on the first page. This allows parallel data on Tn[7:0] to be encoded, serialized, looped back, deserialized, and decoded. This mode is intended for the system to verify functionality of the local VSC7216-01 prior to attempting to establish an external link. The PTXn and RTXn outputs are unaffected by the state of LBENn[1:0].

When LBENn[1:0] = 01, Parallel Loopback mode is selected. The Rn[7:0] outputs are looped back to the Tn[7:0] inputs (see Figure 13). WSENn does not have a loopback source and is internally connected to a logic LOW. KCHAR does not have a loopback source and functions normally. The C/Dn input is obtained by decoding the link status outputs so that either a data character, a special character, or an IDLE (K28.5) character is transmitted. When the link is in the LOS or RESYNC state, C/Dn is asserted, and the data path is set to 0xBC so that an IDLE can be sent. For other link status conditions, C/Dn follows the KCHn status bit, which guarantees that IDLE and special characters are correctly looped back along with normal data. It also has the effect of looping back the received data as a normal data character when a disparity error, out-of-band character, or underflow/overflow link status condition occurs.

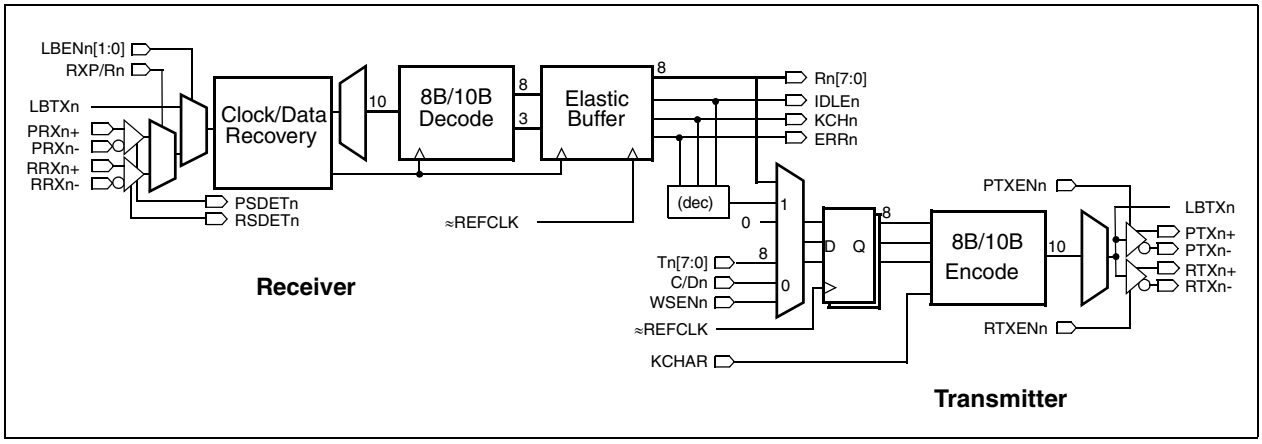


Figure 13. Parallel Loopback Mode Operation

In Parallel Loopback mode, the receiver uses an internal copy of REFCLK as the word clock in each receiver. This data is looped back to the transmitter with TMODE[2:0] internally set to 000, which guarantees that the parallel loopback data to be retransmitted is frequency-locked to the transmitter's REFCLK. However, the parallel output data should be ignored in this mode of operation because the receiver parallel output data timing will not match the normal system timing that is externally selected by RMODE[1:0].

This internal loopback configuration also allows rate matching to be performed in the receivers' elastic buffers. Rate matching is controlled and operates in exactly the same way in normal mode. This rate matching is required in order to avoid receiver overrun/underrun errors in the loopback device if the remote transmitting device's REFCLK is not frequency-locked to the loopback device's REFCLK. Keep in mind that the LBENn[1:0], RXP/Rn, PTXENn, RTXENn, and BIST inputs must be configured appropriately for end-to-end parallel loopback to function correctly in a user environment. Parallel Loopback mode is internally disabled when BIST mode is enabled.

Built-In Self-Test Operation

The Built-In Self-Test (BIST) mode is enabled when the BIST input is HIGH, which causes TMODE[2:0] to be internally set to 000. When the transmitter enters BIST mode, it issues a Word Sync Sequence to recenter the elasticity buffers in the receive channel. Each transmitter then repeatedly sends a simple 256-byte incrementing data pattern (prior to 8B/10B encoding), followed by three IDLE characters (K28.5). Note that this incrementing pattern, plus the three IDLEs, causes transmission of both the disparities of each data character and the disparities of the IDLE character. The pattern also contains a sufficient IDLE density for any application requiring IDLE insertion/deletion. It is up to the user to enable IDLE insertion/deletion if the receiver's word clock is not frequency-locked to the transmitter's reference clock.

Each receiver monitors incoming data for this pattern and indicates if any errors are detected. Correct reception of the pattern is reported on each receiver's TBERRn output: a LOW means the pattern is being received correctly, and a HIGH means that errors are detected. When BIST transitions from LOW to HIGH, each TBERRn output is initialized HIGH. It will be cleared LOW whenever one or more IDLE characters, followed by all 256 data characters, are sequentially received without error, and set HIGH whenever a pattern mismatch or receiver error is encountered. Each channel operates independently and no attempt is made to word-align the receive channels. Received data and associated status is generated the same as in normal operation. Note that Serial Loopback mode and receiver output timing mode selection by means of RMODE[1:0] operate independently of BIST mode; however, BIST mode disables Parallel Loopback mode.

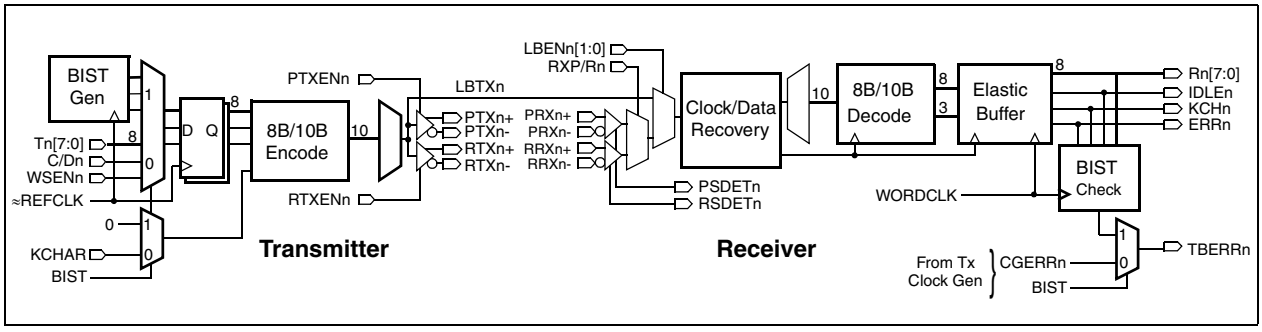


Figure 14. BIST Operation Mode

Compatibility with the VSC7214 and VSC7211

The VSC7216-01's functionality is carefully defined to ensure compatibility with the VSC7211 and VSC7214 at the serial link level, and that the transmitter and receiver low-speed interfaces have compatible modes of operation. It is strongly recommended that the VSC7216-01 not be connected in any way through the WSO and/or WSI pins to a VSC7211 or VSC7214.

Serial Link Compatibility

The VSC7216-01 uses the same Fibre Channel 8B/10B encoding scheme and the same Word Sync Sequence that is used in the VSC7211 and VSC7214. In serial link operation, the only difference between the VSC7216-01 and the VSC7211 and VSC7214 is that the VSC7211 and VSC7214 require four consecutive identically-aligned comma patterns to set the character framing boundary, while the VSC7216-01 requires a single comma. In other words, the VSC7216-01 will make an earlier transition from the LOSS_OF_SYNC state to the RESYNC state (one comma

instead of four), as shown in Figure 11. Once out of the LOSS_OF_SYNC state, there is no difference in receiver behavior in the absence of data link errors. When transmitting in 32-bit mode from VSC7216-01 to VSC7211 or VSC7214, use TMODE[2:0] = 000 or = 1X0 (common transmit interface timing source) to minimize transmitter interchannel skew.

Parallel Interface Compatibility

In general, the VSC7216-01 low-speed parallel interfaces can be configured so that there are input and output signals that are compatible with their VSC7211 and VSC7214 counterparts. On the transmit interface, the signals Tn[7:0] and C/Dn behave identically on the VSC7216-01, as long as the input timing is referenced to REFCLK (that is, TMODE[2:0] = 000). On the receive interface, the signals Rn[7:0], ERRn, KCHn, and IDLEn behave identically on the VSC7216-01, as long as these four receive channels output data that is centered around REFCLK (RMODE[1:0] = 00) or timed to RCLKA/RCLKNA (RMODE[1:0] = 10). When RMODE[1:0] = 10, the VSC7216-01 RCLKn/RCLKNn outputs provide four copies of RCLKA/RCLKNA, which are equivalent to the VSC7211 and VSC7214 RCLK/RCLKN outputs.

The KCHAR input on the VSC7216-01 is no longer a synchronous input timed to REFCLK as on the VSC7211 and VSC7214. It is a static input that is used to define the control character encoding mode when C/Dn = 1, as shown in Table 3. The VSC7216-01 also has a separate WSENn input per channel instead of a common WSYNC input, as on the VSC7211 and VSC7214.

Operational Mode Compatibility

Eight operating modes of the VSC7211 and VSC7214 are defined below and are based on the binary combinations of the RCLKEN, FLOCK, and INDEP inputs. These mode inputs control VSC7211 and VSC7214 receiver operation only and have no effect on transmitter operation. For each of these modes, the equivalent VSC7216-01 receiver configuration is presented.

VSC7214 MODE 0: RCLKEN = LOW, FLOCK = LOW, INDEP = LOW

Receiver Rn[7:0], ERRn, KCHn, and IDLEn outputs are synchronous to REFCLK, IDLE insertion/deletion is enabled, and the receive channels are word-aligned. Configure the VSC7216-01with: RMODE[1:0] = 00, FLOCK = 0, and WSI connected to its own WSO or to the WSO of another VSC7216-01 if multiple devices are used in parallel. The WSI connection allows IDLE insertion/deletion to occur in parallel across all word-aligned channels.

VSC7214 MODE 1: RCLKEN = LOW, FLOCK = LOW, INDEP = HIGH

Receiver Rn[7:0], ERRn, KCHn and IDLEn outputs are synchronous to REFCLK, IDLE insertion/deletion is enabled, and the receive channels are independent. Configure the VSC7216-01 with: RMODE[1:0] = 00, FLOCK = 0, and WSI = 1. The WSI connection inhibits channel alignment and allows IDLE insertion/deletion to occur independently in each channel.

VSC7214 MODE 2: RCLKEN = LOW, FLOCK = HIGH, INDEP = LOW

Receiver Rn[7:0], ERRn, KCHn, and IDLEn outputs are synchronous to REFCLK, IDLE insertion/deletion is disabled, and the receive channels are word-aligned. Configure the VSC7216-01 with: RMODE[1:0] = 00, FLOCK = 1, and WSI connected to its own WSO or to the WSO of another VSC7216-01 if multiple devices are used in parallel. The WSI connection allows word alignment to occur, and the FLOCK connection inhibits IDLE insertion/deletion.

VSC7214 MODE 3: RCLKEN = LOW, FLOCK = HIGH, INDEP = HIGH

Receiver Rn[7:0], ERRn, KCHn, and IDLEn outputs are synchronous to REFCLK, IDLE insertion/deletion is disabled, and the receive channels are independent. Configure the VSC7216-01 with: RMODE[1:0] = 00, FLOCK = 1, and WSI = 0. The WSI connection inhibits channel alignment, and the FLOCK connection inhibits IDLE insertion/deletion.

VSC7214 MODE 4: RCLKEN HIGH, FLOCK = LOW, INDEP = LOW

This configuration does not require IDLE insertion/deletion; use Mode 6.

VSC7214 MODE 5: RCLKEN = HIGH, FLOCK = LOW, INDEP = HIGH

Receiver Rn[7:0], ERRn, KCHn, and IDLEn outputs are synchronous to RCLKn/RCLKNn, IDLE insertion/deletion is enabled, and the receive channels are independent. Configure the VSC7216-01 with: RMODE[1:0] = 10, FLOCK = 0, and WSI = 1. The WSI connection inhibits channel alignment and allows IDLE insertion/deletion to occur independently in each channel. The RCLKn/RCLKNn outputs of Channels B, C, and D are copies of RCLKA/RCLKNA.

VSC7214 MODE 6: RCLKEN = HIGH, FLOCK = HIGH, INDEP = LOW

Receiver Rn[7:0], ERRn, KCHn, and IDLEn outputs are synchronous to RCLKn/RCLKNn, IDLE insertion/deletion is disabled, and the receive channels are word-aligned. Configure the VSC7216-01 with: RMODE[1:0] = 10, FLOCK = 1, and WSI connected to its own WSO. Multiple VSC7216-01 devices should not be used in parallel when the outputs are synchronous to RCLKn/RCLKNn. The WSI connection allows word alignment to occur, and the FLOCK connection inhibits IDLE insertion/deletion.

VSC7214 MODE 7: RCLKEN = HIGH, FLOCK = HIGH, INDEP = HIGH

Receiver Rn[7:0], ERRn, KCHn and IDLEn outputs are synchronous to RCLKn/RCLKNn, IDLE insertion/deletion is disabled, and the receive channels are independent. Configure the VSC7216-01 with: RMODE[1:0] = 10, FLOCK = 1, and WSI = 0. The WSI connection inhibits channel alignment, and the FLOCK connection inhibits IDLE insertion/deletion.

ELECTRICAL SPECIFICATIONS

AC Characteristics

Over Recommended Operating Conditions.

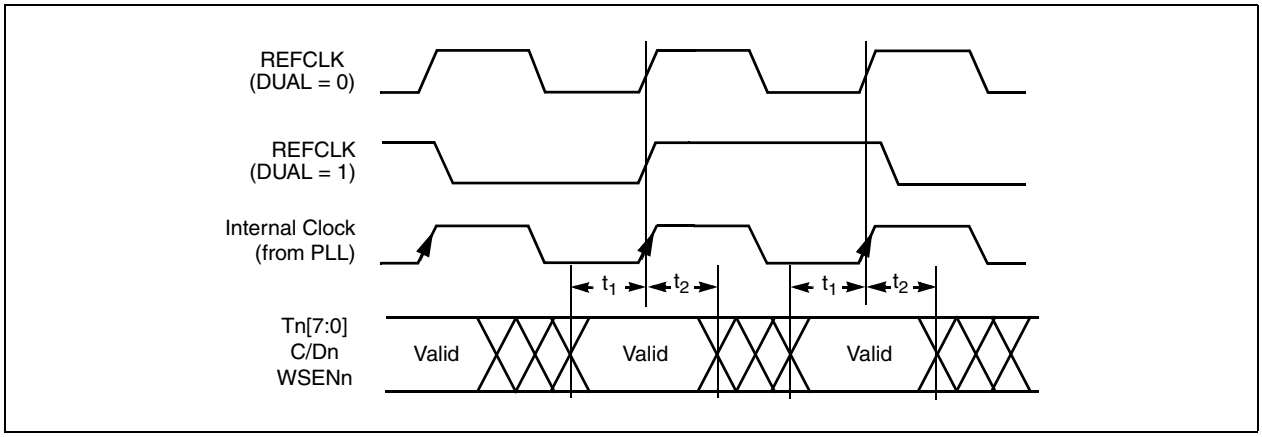


Figure 15. Transmit Input Timing Waveforms With TMODE = 000

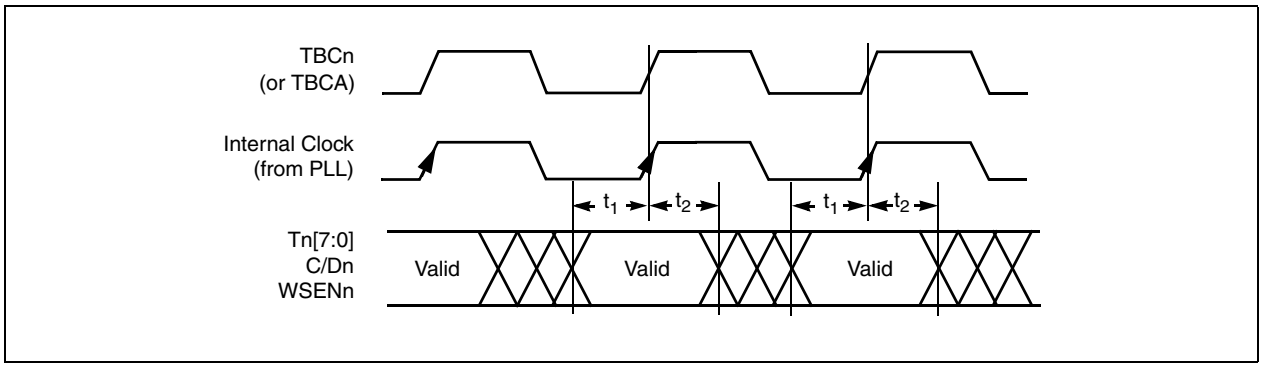


Figure 16. Transmit Input Timing Waveforms With TMODE = 10X

Table 10. Transmit Input AC Characteristics With TMODE = 000 or TMODE = 10X

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_1	Input setup time to the rising edge of REFCLK or TBCn	1.5			ns	Measured between the valid data level of the input and the 1.4V point of REFCLK or TBCn.
t_2	Input hold time after the rising edge of REFCLK or TBCn	1.0			ns	

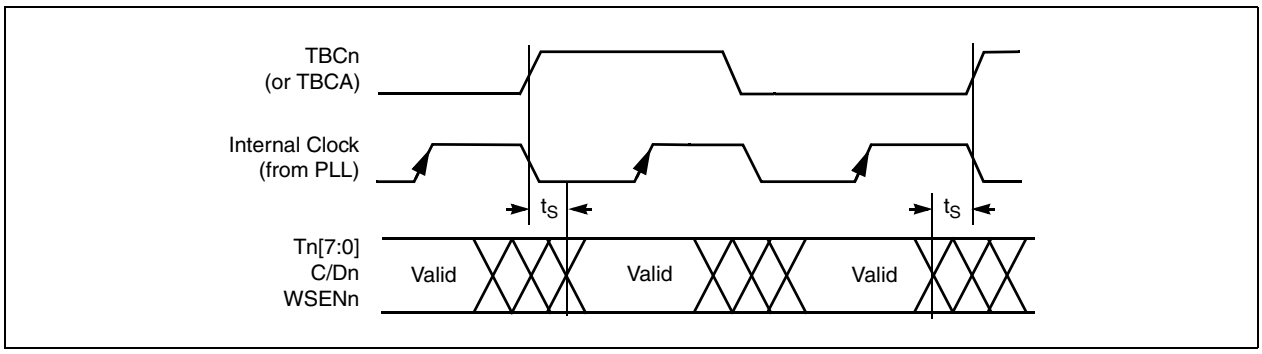


Figure 17. Transmit Input Timing Waveforms With TMODE = 11X (ASIC-Friendly Timing)

Table 11. Transmit Input AC Characteristics With TMODE = 11X

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_S	Input skew relative to the rising edge of TBCn or TBCA			2.0	bc	Measured between the valid data level of the input and the 1.4V point of TBCn or TBCA. bc = bit clock.

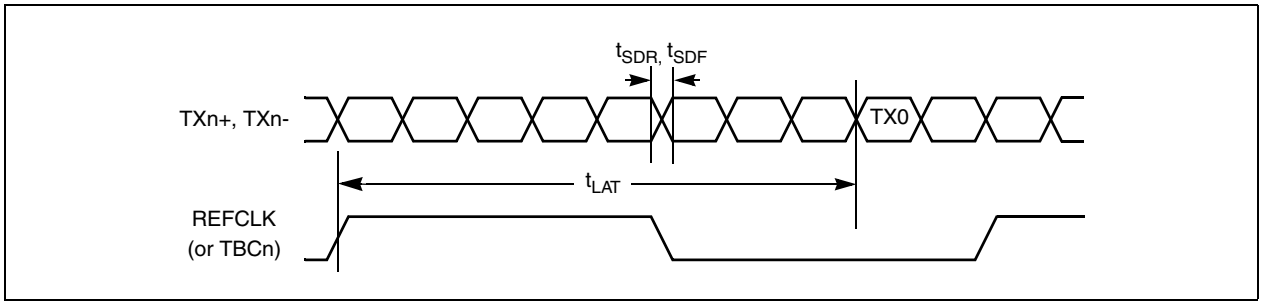


Figure 18. Transmit Serial Timing Waveforms

Table 12. Transmit Serial AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{SDR}, t_{SDF}	TXn+/– rise and fall times			330	ps	Measured between 20% to 80% of the valid data level.
t_{LAT}	Latency, REFCLK to TX0	22bc + 0.1ns		22bc+0.7ns	bc + ns	ENDEC = 1, TMODE = 000
	Latency, TBCA to TX0	38bc + 0.4ns		38bc+0.7ns	bc + ns	ENDEC = 1, TMODE = 10X
	Latency, TBCB/C/D to TX0	32bc + 0.1ns		42bc+0.6ns	bc + ns	ENDEC = 1, TMODE = 101
t_J	Serial data output total jitter (p-p)			192	ps	IEEE 802.3z Clause 38.69. Tested on a sample basis.
t_{DJ}	Serial data output deterministic jitter (p-p)			80	ps	IEEE 802.3z Clause 38.69. Tested on a sample basis.

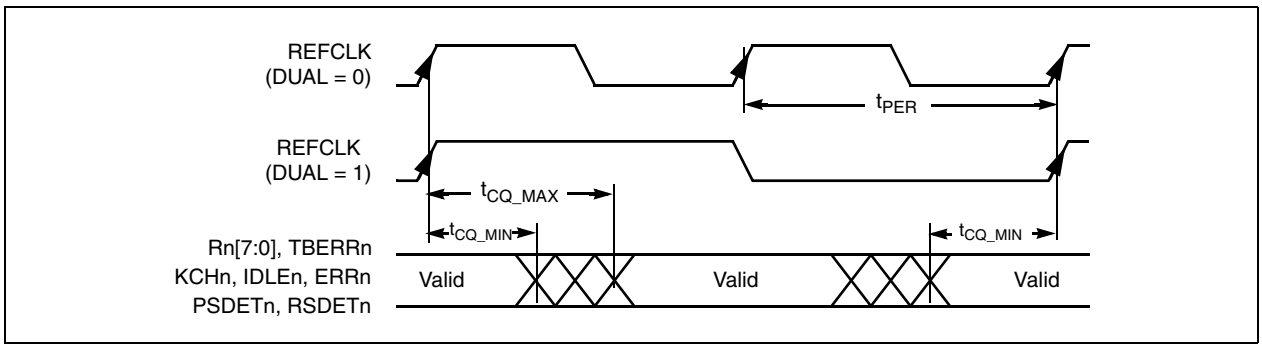


Figure 19. Receive Output Timing Waveforms With RMODE = 00 or 01

Table 13. Receive Output AC Characteristics with RMODE = 00 or 01

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{CQ}	REFCLK rising edge to TTL output transition	2.20ns – 0bc		5.05ns – 0bc	ns	RMODE = 00, bc = bit clock.
t_{CQ}	REFCLK rising edge to TTL output transition	2.20ns – 2bc		5.05ns – 2bc	ns	RMODE = 01, bc = bit clock.
t_{QC}	TTL output transition to REFCLK rising edge	t_{PER} – t_{CQ_MAX}			ns	

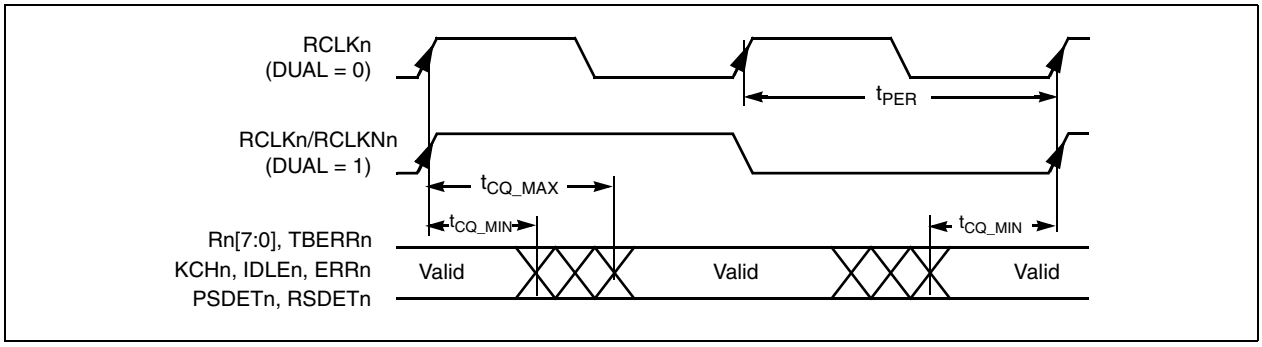


Figure 20. Receive Output Timing Waveforms With RMODE = 10 or 11

Table 14. Receive Output AC Characteristics with RMODE = 10 or 11

Symbol	Parameter	Min	Typ	Max	Units	Condition
t_{CQ}	RCLKn/RCLKNn rising edge to TTL output transition	–1.25ns + 4bc		1.25ns + 4bc	ns	bc = bit clock.
t_{QC}	TTL output transition to RCLKn/RCLKNn rising edge	t_{PER} – t_{CQ_MAX}		t_{PER} – t_{CQ_MIN}	ns	
DC	RCLKn/RCLKNn duty cycle	50% – 1ns		50% + 1ns	ns	Measured at 1.4V.

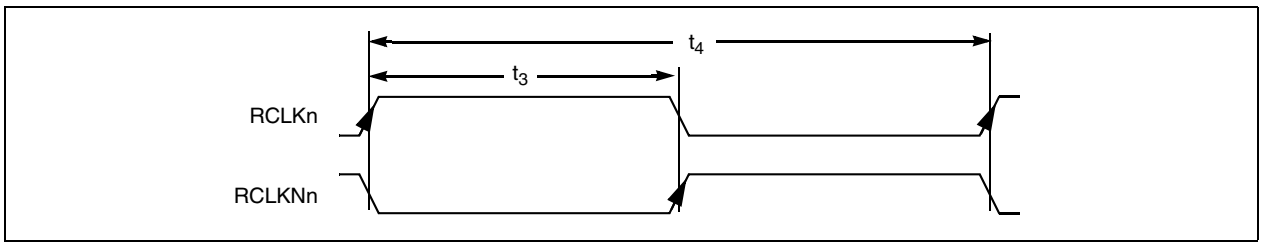


Figure 21. RCLKn and RCLKNn Timing Waveforms With DUAL = 1

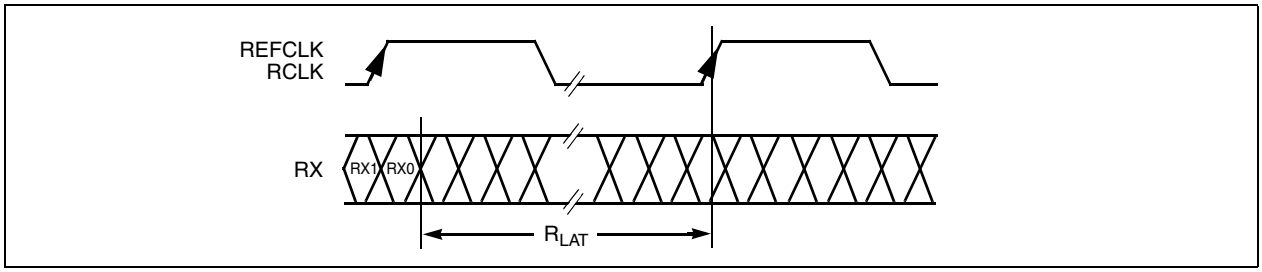


Figure 22. R_{LAT} Timing

Table 15. General Receive AC Characteristics

Symbol	Parameter	Min	Max	Units	Condition
t_3	Delay between rising edge of RCLKn to rising edge of RCLKNn	10 • T_{RX} – 500	10 • T_{RX} + 500	ps	T_{RX} is the bit period of the incoming data on Rx.
Δt_3	RCLKn to RCLKNn skew $Delay = \frac{10}{f_{baud}} \pm \Delta T_3$	–500	+500	ps	Deviation of RCLKn rising edge to RCLKNn rising edge. Nominal delay is 10 bit times.
t_4	Period of RCLKn and RCLKNn	0.99 • t_{REFCLK}	1.01 • t_{REFCLK}	ps	Whether or not locked to serial data, independent of DUAL input.
Δt_4	Deviation of RCLK/RCLKN period from REFCLK period $t_{RCLK} = t_{REFCLK} \pm \Delta t_4$	–1.0	+1.0	%	Whether or not locked to serial data, independent of DUAL input.
t_R, t_F	RCLK output rise and fall times		2.4	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$ into 10pF load.
R_{LAT}	Latency from RX0 to REFCLK or RCLK	70.5bc –1.6ns 48.5bc – 1.6ns	81.5bc + 4.1ns 102.5bc + 4.1ns	bc + ns	ENDEC = 1, recenter only. ENDEC = X, recenter + drift.
t_{LOCK}	Data acquisition lock time(1)		2500	bc	Using K28.5+/K28.5– pattern. Tested on a sample basis.
T_{JTD}	Receive data total jitter tolerance (p-p)		600	ps	IEEE 802.3z Clause 38.69. Tested on a sample basis.
D_{JTD}	Receive data deterministic jitter tolerance (p-p)		370	ps	IEEE 802.3z Clause 38.69. Tested on a sample basis.

1. *The probability of correct data acquisition and recovery is 95% per FC-PH 4.3 Section 5.3.*

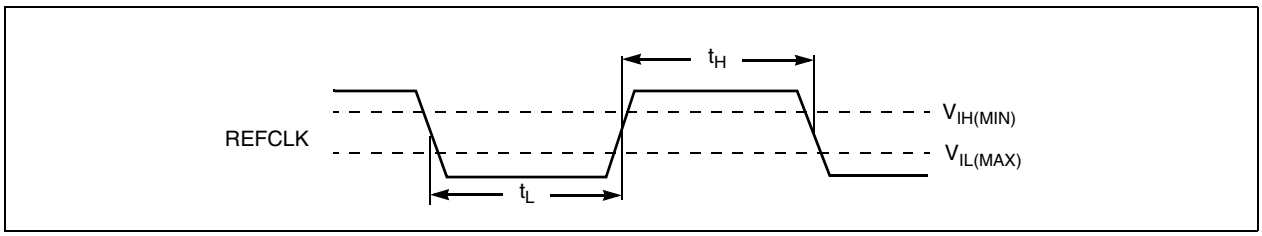


Figure 23. REFCLK Timing Waveform

Table 16. Reference Clock Requirements

Symbol	Parameter	Min	Typ	Max	Unit	Condition
FR	Frequency range	98		136	MHz	DUAL = 0, RATE = 1
		49		68	MHz	DUAL = 1, RATE = 1
		49		68	MHz	DUAL = 0, RATE = 0
		24.5		34	MHz	DUAL = 1, RATE = 0
FO	Frequency offset	–200		+200	ppm	| REFCLK (Tx) – REFCLK (Rx) | = maximum offset between Tx and Rx device. REFCLK's on one serial link
DC	REFCLK duty cycle	35		65	%	Measured at 1.4V.
t_H, t_L	REFCLK and TBC pulse width	3			ns	
t_{RCR},t_{RCF}	REFCLK rise and fall times			1.5	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$.
$REFCLK_{JITTER}$	REFCLK jitter power			100	ps	Peak-to-peak jitter at VSC7216-01's REFCLK input between 100Hz and 3MHz.

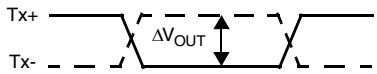
DC Characteristics

Over Recommended Operating Conditions.

Table 17. DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Condition
TTL Outputs: Rn[7:0], KCHn, IDLEn, ERRn, RCLKn/RCLKNn, TBERRn, PSDETn, RSDETn, WSO						
V_{OH}	TTL output HIGH voltage	2.4			V	I_{OH} = –1.0mA
V_{OL}	TTL output LOW voltage			0.5	V	I_{OL} = +1.0mA
I_{OZ}	TTL output leakage current			500	µA	When set to high impedance state through JTAG.
TTL Inputs: TBCn, Tn[7:0], C/Dn, WSENn, KCHAR, RATE, BIST, LBENn[1:0], TMODE[2:0], RMODE[1:0], DUAL, PTXENn, RTXENn, RXP/Rn, RESETN, ENDEC, WSI, FLOCK, TRSTN, TDI, TDO, TMS, TCK						
V_{IH}	TTL input HIGH voltage	2.0		5.5	V	
V_{IL}	TTL input LOW voltage	0		0.8	V	
I_{IH}	TTL input HIGH current		50	500	µA	V_{IN} = 2.4V
I_{IL}	TTL input LOW current			–1000	µA	V_{IN} = 0.5V
PECL Inputs: REFCLKP/REFCLKN						
V_{IH}	PECL input HIGH voltage	V_{DD} – 1.1		V_{DD} – 0.7	V	
V_{IL}	PECL input LOW voltage	V_{DD} – 2.0		V_{DD} – 1.5	V	
I_{IH}	PECL input HIGH current			200	µA	$V_{IN} = V_{IH(MAX)}$
I_{IL}	PECL input LOW current	–50			µA	$V_{IN} = V_{IL(MIN)}$
ΔV_{IN}	PECL input peak-to-peak voltage swing	200			mV	
V_{CM}	PECL input common-mode voltage	V_{DD} – 1.5		V_{DD} – 0.7	V	
V_{BIAS}	REFCLKP/REFCLKN internal input bias voltage		$V_{DD}/2$		V	
PECL Outputs: PTXn+/–, RTXn+/–						
ΔV_{OUT}	PECL peak-to-peak output voltage swing[1]	500		1100	mV	100Ω differential load.
PECL Inputs: PRXn+/–, RRXn+/–						
ΔV_{IN}	PECL peak-to-peak input voltage swing[1]	200		1300	mV	
Miscellaneous						
P_D	Power dissipation		3.0	3.2	W	Maximum at 3.47V, at 130MHz, redundant I/O off. Typical at 3.3V, outputs open.
I_{DD}	Power supply current		910	925	mA	

1. *Single-ended, peak-to-peak measurement results are stated. Differential techniques used in Fibre Channel yield values that are twice the magnitude. See following diagram:*



Recommended Operating Conditions

Table 18. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{DDx}	Power supply voltage	3.14	3.3	3.47	V	
T	Operating temperature range[1]	0		+95	°C	

1. Lower limit of specification is ambient temperature and upper limit is case temperature.

Absolute Maximum Ratings

Table 19. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Condition
V_{DDxx}	Power supply voltage	–0.5	+3.8	V	
	Input voltage, PECL	–0.5	V_{DD} + 0.5	V	
	Input voltage, TTL	–0.5	+5.5	V	
	Output voltage, TTL	–0.5	V_{DD} + 0.5	V	
	Output current, TTL		50	mA	
	Output current, PECL		50	mA	
T_C	Case temperature under bias	–55	+125	°C	
T_S	Storage temperature	–65	+150	°C	
V_{ESD}	ESD voltage (Human Body Model)	–3000	+3000	V	

Stresses listed under Absolute Maximum Ratings may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE

This device can be damaged by ESD. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

PACKAGE INFORMATION

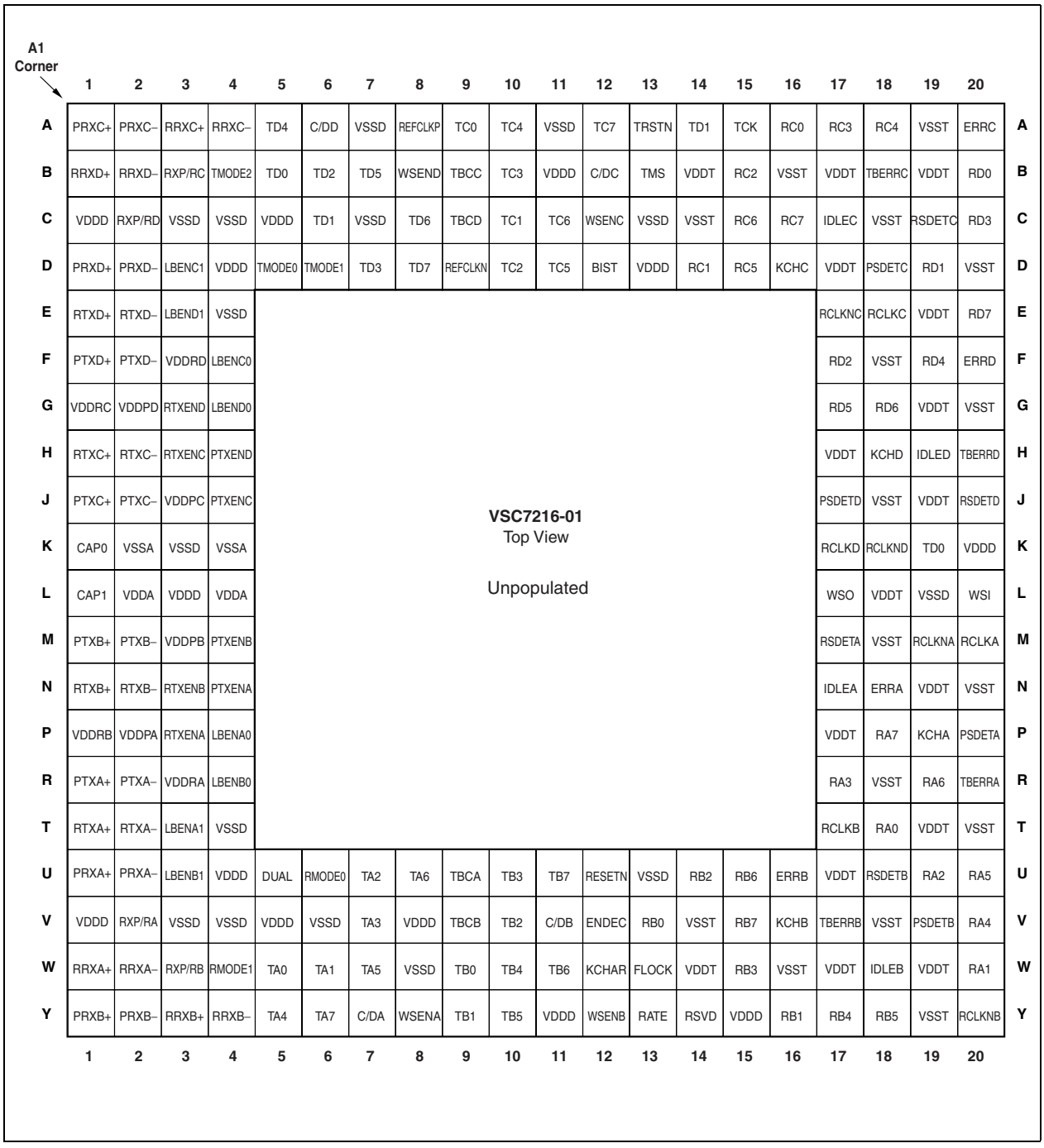


Figure 24. Pin Diagram for 256-Pin BGA (UC)

Table 20. Pin Identification for 256-Pin BGA (UC and UI)

Pin	Name	I/O	Type	Description
6Y, 8U, 7W, 5Y, 7V, 7U, 6W, 5W	TA[7:0]	I	TTL	Transmit Data for Channel n, Synchronous to REFCLK, TBCA or TBCn.
11U, 11W, 10Y, 10W, 10U, 10V, 9Y, 9W	TB[7:0]	I	TTL	Transmit Data for Channel n, Synchronous to REFCLK, TBCB or TBCn.
12A, 11C, 11D, 10A, 10B, 10D, 10C, 9A	TC[7:0]	I	TTL	Transmit Data for Channel n, Synchronous to REFCLK, TBCC or TBCn.
8D, 8C, 7B, 5A, 7D, 6B, 6C, 5B	TD[7:0]	I	TTL	Transmit Data for Channel n, Synchronous to REFCLK, TBCD or TBCn.
7Y 11V 12B 6A	C/DA C/DB C/DC C/DD	I	TTL	Control/Data for Channel n. If KCHAR = C/Dn = LOW, then Tn[7:0] is used to generate transmit data. If KCHAR = C/Dn = HIGH, then special Kxx.x characters are transmitted based upon the value of Tn[7:0]. If KCHAR = LOW and C/Dn = HIGH, IDLE characters are transmitted. When ENDEC = LOW, this is equivalent to data bit Tn8.
8Y 12Y 12C 8B	WSENA WSENB WSENC WSEND	I	TTL	Word Sync Enable for Channel n. Asserted HIGH for one cycle to initiate transmission of the Word Sync Sequence as defined in Figure 5 and related text. When ENDEC = LOW, this is equivalent to data bit Tn9.
9U 9V 9B 9C	TBCA TBCB TBCC TBCD	I	TTL	Transmit Byte Clock for Channel n. Optional input data timing reference for Tn[7:0], WSENn and C/Dn.
12W	KCHAR	I	TTL	Special Kxx.x Character Enable. When C/Dn is HIGH, KCHAR controls data sent to the transmitter. When LOW, IDLE characters are sent. When HIGH, special Kxx.x characters are sent as encoded on Tn[7:0]. This is intended to be a static input and cannot be changed on a cycle-by-cycle basis. When ENDEC = LOW, this is equivalent to ENCDET.
5D 6D 4B	TMODE0 TMODE1 TMODE2	I	TTL	Transmit Input Data Timing Mode. Determines the timing reference for Tn[7:0], WSENn, and C/Dn on all channels as defined in Table 2.
20R 17V 18B 20H	TBERRA TBERRB TBERRC TBERRD	O	TTL	Transmit Buffer Error for Channel n. When HIGH, indicates that the elastic limit of the transmit input skew buffer was exceeded. Output timing is the same as Rn[7:0]. A LOW indicates correct reception of the 256-byte incrementing pattern in BIST mode.
1R, 2R 1M, 2M 1J, 2J 1F, 2F	PTXA+/– PTXB+/– PTXC+/– PTXD+/–	O	PECL	Primary Differential Serial TX Outputs for Channel n. These pins output serialized transmit data when PTXENn is HIGH. When PTXENn is LOW, these output buffers are powered down, the pin is undriven, and both pins (+/–) float to an unknown HIGH state (~ +1.8V). AC-coupling is recommended. External pull-down resistors are not required.
1T, 2T 1N, 2N 1H, 2H 1E, 2E	RTXA+/– RTXB+/– RTXC+/– RTXD+/–	O	PECL	Redundant Differential Serial TX Outputs for Channel n. These pins output serialized transmit data when RTXENn is HIGH. When RTXENn is LOW, these output buffers are powered down, the pin is undriven, and both pins (+/–) float to an unknown HIGH state (~ +1.8V). AC-coupling is recommended. External pull-down resistors are not required.

Table 20. Pin Identification for 256-Pin BGA (UC and UI)

Pin	Name	I/O	Type	Description
4N 4M 4J 4H	PTXENA PTXENB PTXENC PTXEND	I	TTL	Primary TX Output Enable for Channel n. When HIGH, PTXn+/– is active, and when LOW PTXn+/– is powered down, and the outputs are undriven.
3P 3N 3H 3G	RTXENA RTXENB RTXENC RTXEND	I	TTL	Redundant TX Output Enable for Channel n. When HIGH RTXn+/- is active, and when LOW, RTXn+/– is powered down, and the outputs are undriven.
18P, 19R 20U, 20V 17R, 19U 20W, 18T	RA[7:0]	O	TTL	Receive Data for Channel A. Synchronous to RCLKA/RCLKNA or REFCLK as selected by RMODE[1:0].
15V, 15U 18Y, 17Y 15W, 14U 16Y, 13V	RB[7:0]	O	TTL	Receive Data for Channel B. Synchronous to RCLKB/RCLKNB or REFCLK as selected by RMODE[1:0].
16C, 15C 15D, 18A 17A, 15B 14D, 16A	RC[7:0]	O	TTL	Receive Data for Channel C. Synchronous to RCLKC/RCLKNC or REFCLK as selected by RMODE[1:0].
20E, 18G 17G, 19F 20C, 17F 19D, 20B	RD[7:0]	O	TTL	Receive Data for Channel D. Synchronous to RCLKD/RCLKND or REFCLK as selected by RMODE[1:0].
17N 18W 17C 19H	IDLEA IDLEB IDLEC IDLED	O	TTL	IDLE Detect for Channel n. When HIGH, an IDLE character has been detected by the decoder and is on Rn[7:0]. When ENDEC = LOW, this is equivalent to COMDETn.
19P 16V 16D 18H	KCHA KCHB KCHC KCHD	O	TTL	Kxx.x Character Detect for Channel n. When HIGH, a special Kxx.x character has been detected on Rn[7:0] by the decoder. When ENDEC = LOW, this is equivalent to data bit Rn8.
18N 16U 20A 20F	ERRA ERRB ERRC ERRD	O	TTL	Error Detect for Channel n. When HIGH, an invalid 10-bit character or disparity error has been detected, and the data on Rn[7:0] is invalid. When ENDEC = LOW, this is equivalent to data bit Rn9.
20M 19M 17T 20Y 18E 17E 17K 18K	RCLKA RCLKNA RCLKB RCLKNB RCLKC RCLKNC RCLKD RCLKND	O	TTL	Recovered Clock Outputs for Channel n. These outputs are driven from either the channel A or channel n recovered clock at $1/10^{th}$ or $1/20^{th}$ the baud rate, as selected by RMODE[1:0] and DUAL. When unused and REFCLK is selected as the output timing reference, RCLKn is LOW and RCLKNn is HIGH.
6U 4W	RMODE0 RMODE1	I	TTL	Receive Output Data Timing Mode. Determines the timing reference for all receive channels' Rn[7:0], IDLEn, KCHn, and ERRn output data and for the PSDETn, RSDETn and TBERRn outputs, as defined in Table 6.
1U, 2U 1Y, 2Y 1A, 2A 1D, 2D	PRXA+/- PRXB+/- PRXC+/- PRXD+/-	I	PECL	Primary Differential Serial Rx Inputs for Channel n. These pins receive the serialized input data when LBENn[1] is LOW and RXP/Rn is HIGH (see Table 5 and Table 9). These pins are internally biased at $V_{DD}/2$ through a 3.2kΩ resistor to the bias voltage. AC-coupling is recommended.

Table 20. Pin Identification for 256-Pin BGA (UC and UI)

Pin	Name	I/O	Type	Description
1W, 2W 3Y, 4Y 3A, 4A 1B, 2B	RRXA+/- RRXB+/- RRXC+/- RRXD+/-	I	PECL	Redundant Differential Serial Rx Inputs for Channel n. These pins receive the serialized input data when LBENn[1] is LOW (see Table 5 and Table 9) and RXP/Rn is LOW. These pins are internally biased at $V_{DD}/2$ through a 3.2kΩ resistor to the bias voltage. AC-coupling is recommended.
4P 3T 4R 3U 4F 3D 4G 3E	LBENA0 LBENA1 LBENB0 LBENB1 LBENC0 LBENC1 LBEND0 LBEND1	I	TTL	Loop Back Enable for Channel n. These inputs control the channel serial or parallel loopback configuration as described in Table 9.
2V 3W 3B 2C	RXP/RA RXP/RB RXP/RC RXP/RD	I	TTL	Rx Input Primary/Redundant Serial Input Select for Channel n. When LBENn(1) is LOW, HIGH on RXP/Rn selects PRXn serial input and LOW selects RRXn serial input (see Table 5 and Table 9).
20P 19V 18D 17J	PSDETA PSDETB PSDETC PSDETD	O	TTL	Primary Analog Signal Detect, Channel n. This output goes HIGH when the amplitude on PRXn is greater than 200mV and LOW when the input is less than 80mV. PSDETn is not defined when the input is between 80mV and 200mV. Output timing is same as Rn[7:0].
17M 18U 19C 20J	RSDETA RSDETB RSDETC RSDETD	O	TTL	Redundant Analog Signal Detect, Channel n. This output goes HIGH when the amplitude on RRXn is greater than 200mV and LOW when the input is less than 80mV. RSDETn is not defined when the input is between 80mV and 200mV. Output timing is same as Rn[7:0].
8A 9D	REFCLKP REFCLKN	I	PECL	REFCLK Differential Positive and Negative PECL or Single-Ended TTL Inputs. This rising edge of this clock latches transmit data and control into the input register. It also provides the reference clock at $1/10^{th}$ or $1/20^{th}$ of the baud rate to the PLL, as selected by DUAL. For PECL, connect both REFCLKP and REFCLKN. If TTL, connect to REFCLKP.
1K 1L	CAP0 CAP1		Analog	Loop Filter Capacitor for Clock Generation PLL. These pins must be properly connected to external capacitors, typically 0.1µF. See "Clock Synthesizer" and Figure 1 for more details.
5U	DUAL	I	TTL	Dual Clock Mode. When LOW, REFCLK and RCLKn/RCLKNn are $1/10^{th}$ the baud rate. When HIGH, they are $1/20^{th}$ the baud rate.
13W	FLOCK	I	TTL	Frequency-Locked Mode. When HIGH, each transmit channel's REFCLK is frequency-locked to the receive channel's word clock. When LOW, rate matching can be enabled; however, it is also dependent on WSI input per Table 7.
12D	BIST	I	TTL	Built-In Self-Test Mode. When HIGH, all transmit channels continuously send a 256-byte incrementing data pattern, and all receive channels signal correct reception of the test pattern with a LOW on the TBERRn outputs. When LOW, BIST mode is disabled.
12V	ENDEC	I	TTL	Encoder/Decoder Enable. When HIGH, the VSC7216-01 is configured for 8-bit operation, and internal 8B/10B encoding is enabled. When LOW, a 10-bit interface is used, and internal 8B/10B encoding is bypassed.
12U	RESETN	I	TTL	RESETN Input. When asserted LOW, the transmitter input skew buffers and receiver elastic buffers are recentered.
20L	WSI	I	TTL	Word Sync Input. Used to control channel alignment and IDLE character insertion/deletion, as defined in Table 7.

Table 20. Pin Identification for 256-Pin BGA (UC and UI)

Pin	Name	I/O	Type	Description
17L	WSO	O	TTL	Word Sync Output. Used to set initial channel word alignment and to maintain alignment by controlling IDLE character insertion/deletion, as defined in Table 7.
15A	TCK	I	TTL	JTAG Test Access Port Test Clock Input.
13B	TMS	I	TTL	JTAG Test Access Port Test Clock Input.
14A	TDI	I	TTL	JTAG Test Access Port Test Clock Input.
19K	TDO	O	TTL	JTAG Test Access Port Test Data Output.
13A	TRSTN	I	TTL	JTAG Test Access Port Test Logic Reset Input.
14Y	RSVD		N/A	Reserved Input for future use. Set HIGH for compatibility reasons.
13Y	RATE	I	TTL	Rate Mode. When HIGH, VSC7216-01 runs at full data rate. When LOW, half-speed data rate is selected.
2L, 4L	VDDA	Pwr		Analog Power Supply to PLL. Filter with a ferrite bead and decoupling capacitors to VSSA.
2K, 4K	VSSA	Pwr		Analog ground to PLL.
11B, 11Y, 13D, 15Y, 1C, 1V, 20K, 3L, 4D, 4U, 5C, 5V, 8V	VDDD	Pwr		Digital power supply.
11A, 13C, 13U, 19L, 3C, 3K, 3V, 4C, 4E, 4T, 4V, 6V, 7A, 7C, 8W	VSSD	Pwr		Digital ground.
14B, 14W, 17B, 17D, 17H, 17P, 17U, 17W, 18L, 19B, 19E, 19G, 19J, 19N, 19T, 19W	VDDT	Pwr		TTL output power supply.
14C, 14V, 16B, 16W, 18C, 18F, 18J, 18M, 18R, 18V, 19A, 19Y, 20D, 20G, 20N, 20T	VSST	Pwr		TTL output ground.

Table 20. Pin Identification for 256-Pin BGA (UC and UI)

Pin	Name	I/O	Type	Description
2P	VDDPA	Pwr		PECL output power supply for PTXA.
3R	VDDRA			PECL output power supply for RTXA.
3M	VDDPB			PECL output power supply for PTXB.
1P	VDDRB			PECL output power supply for RTXB.
3J	VDDPC			PECL output power supply for PTXC.
1G	VDDRC			PECL output power supply for RTXC.
2G	VDDPD			PECL output power supply for PTXD.
3F	VDDRD			PECL output power supply for RTXD.
				Leave the power supply pin open if the use of an output is not required.

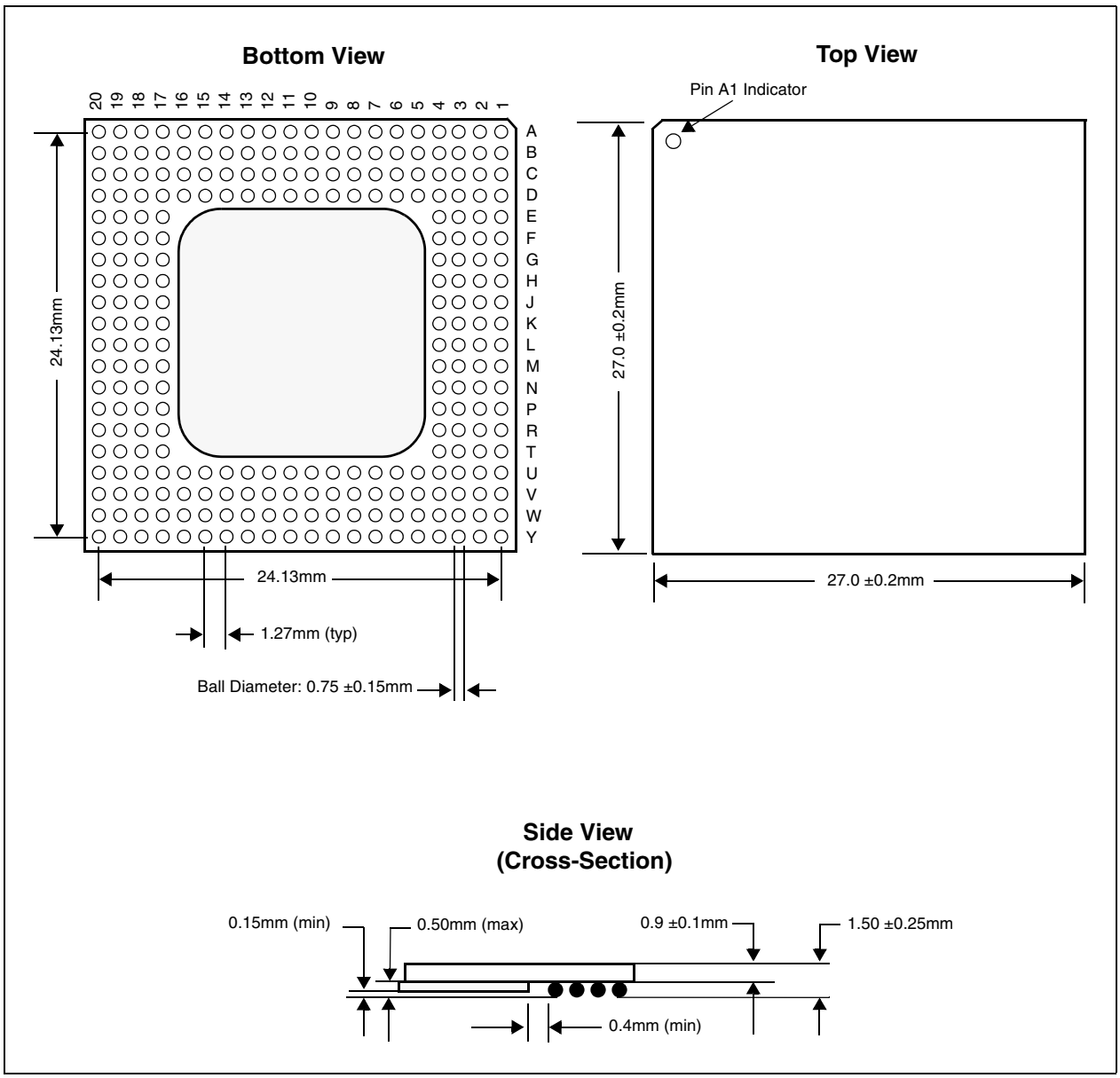


Figure 25. Package Drawing for 256-Pin BGA, 27mm x 27mm x 1.27mm (UC)

The VSC7216-01 is packaged in a 256-pin, thermally enhanced BGA in a 20x20 array, which offers excellent electrical characteristics, good thermal performance, and small size. This package uses an industry-standard footprint. The package construction is shown in Figure 26.

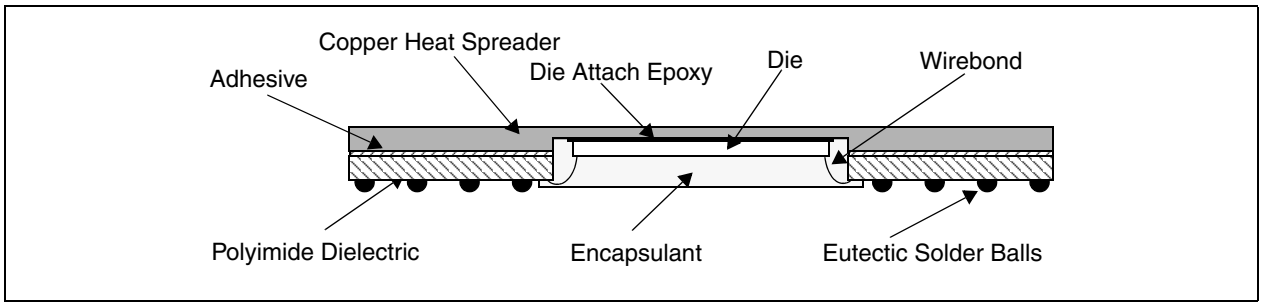


Figure 26. Package Cross Section

Moisture Sensitivity Level

This device is rated moisture sensitivity level 3 or better as specified in JEDEC standard IPC/JEDEC J-STD-020B. For more information, see the JEDEC standard.

ORDERING INFORMATION

VSC7216-01 Multi-Gigabit Interconnect Chip

Part Number	Description
VSC7216UC-01	256-pin BGA, 27mm x 27mm x 1.27mm body

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