P160
Communications Module
User Guide

Version 2.0
December 2002

PN# DS-MANUAL-MBEXP1

Memec Design

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Tables

1 Overview

The P160 Communications Module provides a useful set of peripherals and memory banks in a small, low cost daughter card form-factor, compatible with any main system board containing the P160 expansion interface. The Spartan-II, Spartan-IIE, and Virtex-II system boards from Memec Design all include the P160 interface and can support the P160 Communications Module. If you are planning on using the P160 module with the Memec Design Virtex-II Pro board, you should verify that you have a Rev 2 version of the P160 Communications module. The Rev 2 module contains its own JTAG header and does not share the JTAG chain of the system board. Only the Memec Design Virtex-II Pro board requires this due to a special 2.5V JTAG chain.

Proper user configuration of the main system board is required to enable the P160 interface and the corresponding expansion module functions. This user guide helps provide the necessary details to develop such a configuration. Complete board schematics are provided in Appendix A for your reference.

2 The P160 Communications Module Board

The P160 Communications Module includes interfaces for USB, 10/100 Ethernet, RS-232, PS/2 Keyboard, I2C, SPI, and an LCD display. The module also contains both 2M x 32 Flash and 256K x 32 SRAM. Figure 1 shows the module and its corresponding components, while Figure 2 illustrates the functional block diagram.

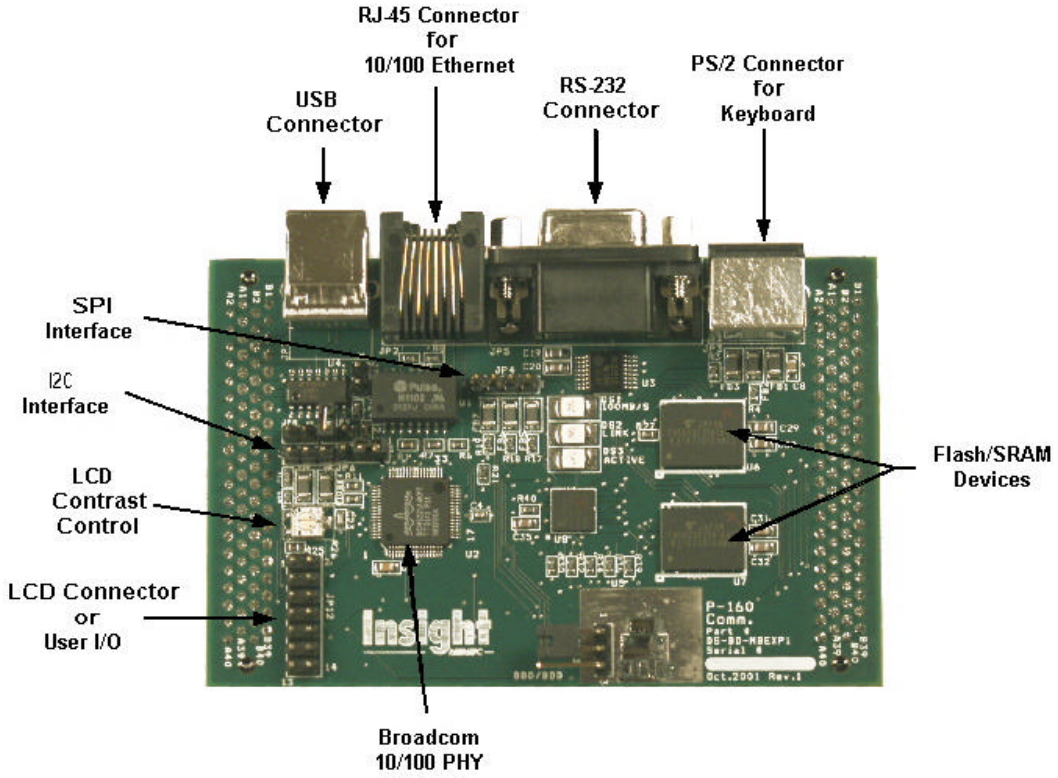

Figure 1 – P160 Communications Module Board

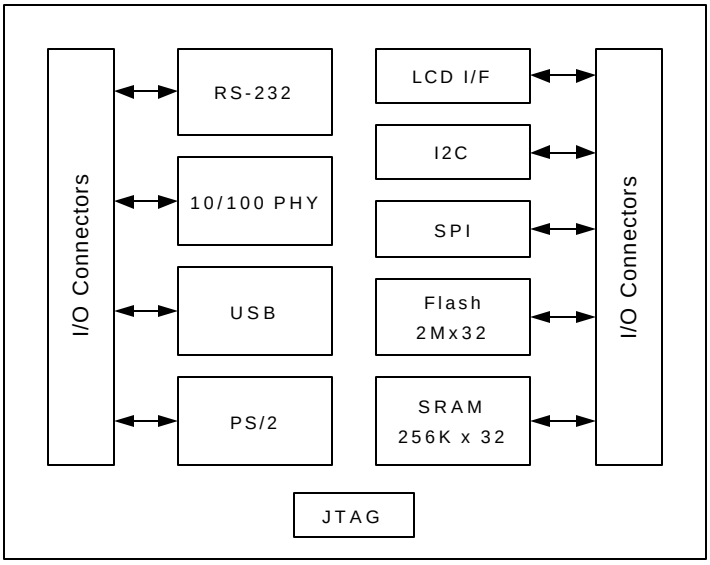

Figure 2 – P160 Communication Module Block Diagram

2.1 10/100 Ethernet

The P160 Communications Module provides a 10/100 Ethernet PHY interface. The Broadcom BCM5221 implements the PHY function while the 10/100 Ethernet core must reside on the main system board, usually inside the FPGA device. The following figure shows a high-level block diagram of the 10/100 interface on the P160 Communications Module.

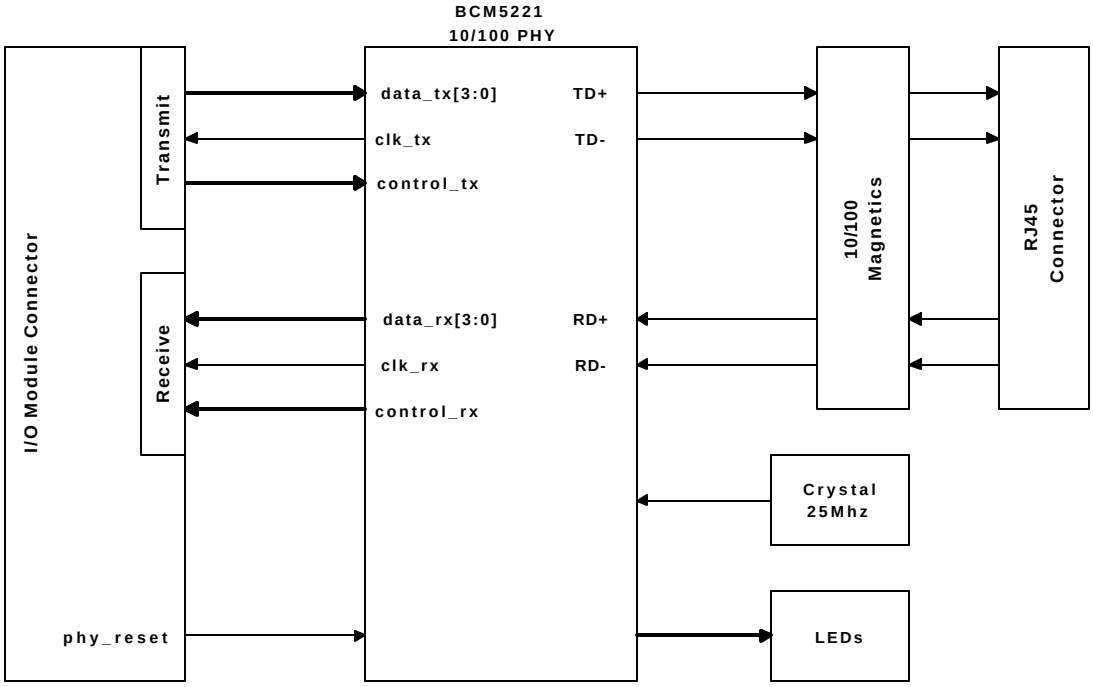

Figure 3 – 10/100 Ethernet Interface

Table 1 – Ethernet Pin Assignments

Signal Name	JX1 Pin #	FPGA I/O/B
PHY_RESETn	B31	O
ETH_MDIO	A13	B
ETH_MDC	B14	O
ETH_COL	B24	I
ETH_CRS	B25	I
ETH_TXD0	A21	O
ETH_TXD1	B22	O
ETH_TXD2	B23	O
ETH_TXD3	A23	O
ETH_TXEN	B21	O
ETH_TXC	A35	I
ETH_TXER	A19	O
ETH_RXD0	B17	I
ETH_RXD1	B16	I
ETH_RXD2	A15	I
ETH_RXD3	B15	I
ETH_RXDV	A17	I
ETH_RXC	A33	I
ETH_RXER	B19	I

2.2 USB Port

The P160 Communications Module provides a USB transceiver interface that can be used for USB end-point applications (USB master applications are not supported on this module). The P160 module utilizes the Fairchild USB1T11A device to implement the transceiver function while the USB core must reside in the FPGA on the main system board. Figure 4 shows a high-level block diagram of the USB interface.

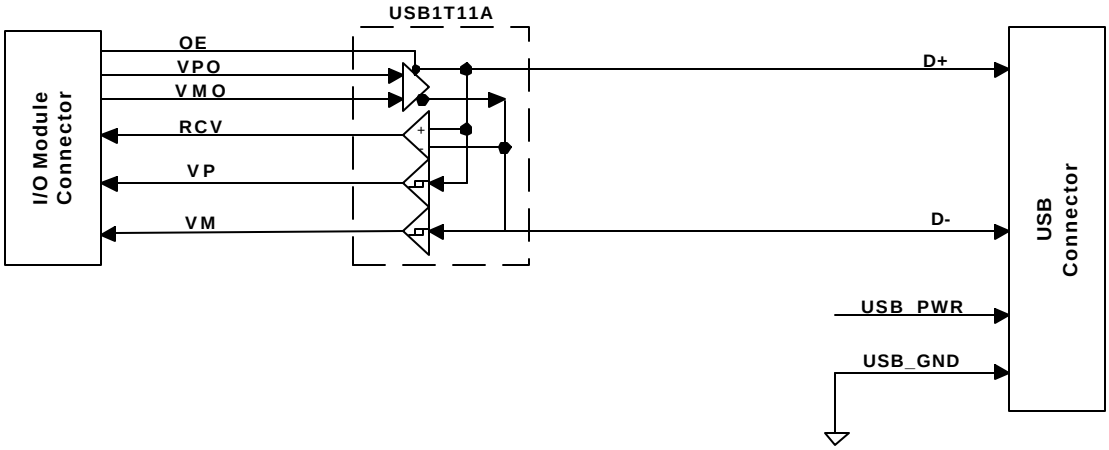

Figure 4 – USB Interface

2.3 RS232 Port

The P160 Communications Module provides a simple RS232 port. This board utilizes the TI MAX3221 RS232 driver for driving the RD and TD signals. Figure 4 shows the RS232 interface.

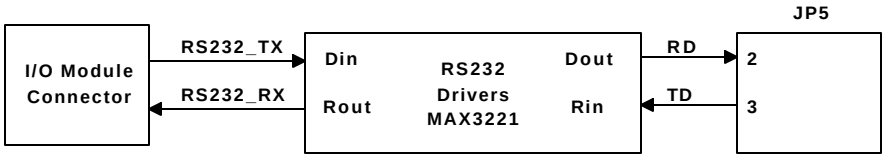

Figure 5 – RS232 Interface

Table 2 – RS232 Pin Assignments

JX1 Pin #	Signal Name	JP5 Pin #
B12	RS232_TX	2
B13	RS232_RX	3

2.4 I2C Port

The P160 Communications Module provides one I2C port. Please refer to the P160 module connector pin assignments and schematics for more information on these signals.

Table 3 – I2C JP6 Pin Assignments

JP6 Pin #	Signal Name
1	I2C_DATA
2	I2C-CLK
3	GND

2.5 SPI Port

The P160 Communications module provides one SPI port. Please refer to the P160 module connector pin assignments and schematics for more information on these signals.

Table 4 – SPI JP4 Pin Assignments

JP4 Pin #	Signal Name
1	SPI_CLK
2	SPI_OUT
3	SPI_IN
4	GND

2.6 FLASH and SRAM

The P160 Communications Module provides 8MB of Flash (2M x 32). Two Toshiba TH50VSF2581 devices (2M x 16 each) are used to achieve this density. In addition to the Flash, these two devices provide 1MB of SRAM. The following figure shows the Flash/SRAM interface on the I/O module.

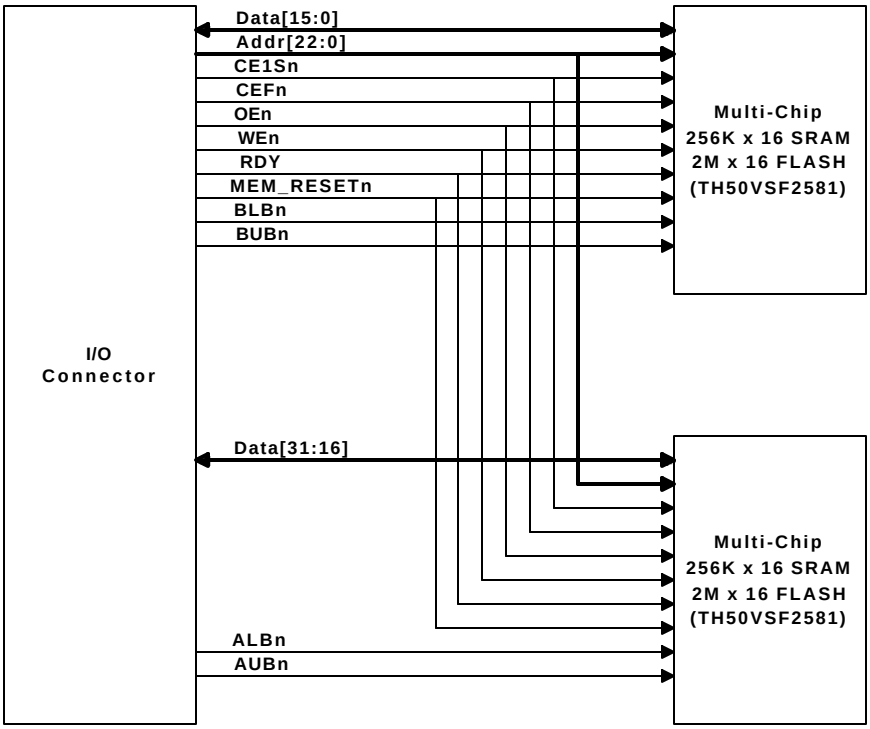

Figure 6 – Flash and SRAM Interface

Table 5 – Flash/SRAM JX Pin Assignments

Signal Name	JX Pin #	FPGA I/O/B
MEM_RESETn	JX1-B37	O
MEM.RY/BY	JX2-A39	I
MEM.AUBn	JX1-A27	O
MEM.BUBn	JX1-B27	O
MEM.ALBn	JX1-A25	O
MEM.BLBn	JX1-B26	O
MEM.WEn	JX2-A40	O
MEM.OEn	JX2-A19	O
MEM.CEFn	JX2-B20	O
MEM.CE1Sn	JX2-A20	O
MEM_DU	JX1-B38	O
A0	JX2-B32	O
A1	JX2-A34	O
A2	JX2-A35	O
A3	JX2-B36	O
A4	JX2-A33	O
A5	JX2-A36	O
A6	JX2-A37	O
A7	JX2-A38	O
A8	JX2-A1	O
A9	JX2-A3	O
A10	JX2-B6	O
A11	JX2-B2	O

A12	JX2-A4	O
A13	JX2-A5	O
A14	JX2-A8	O
A15	JX2-B4	O
A16	JX2-B8	O
A17	JX2-B34	O
A18	JX2-B38	O
A19	JX2-A2	O
A20	JX2-B40	O
A21	JX2-A6	O
A22	JX2-A7	O
D0	JX2-A18	B
D1	JX2-A21	B
D2	JX2-A17	B
D3	JX2-B14	B
D4	JX2-A13	B
D5	JX2-A14	B
D6	JX2-A9	B
D7	JX2-A11	B
D8	JX2-B18	B
D9	JX2-A16	B
D10	JX2-B16	B
D11	JX2-A15	B
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D15	JX2-A10	B
D16	JX2-B30	B
D17	JX2-A32	B
D18	JX2-B28	B
D19	JX2-A27	B
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D24	JX2-A30	B
D25	JX2-A31	B
D26	JX2-A29	B
D27	JX2-A28	B
D28	JX2-A25	B
D29	JX2-A24	B
D30	JX2-B24	B
D31	JX2-B22	B

2.7 PS/2 Keyboard Interface

The P160 module provides standard PS/2 keyboard connector (JP3) for connecting a PS/2 compatible keyboard. The signals present on JP3 are not driven directly from the P160 connectors JX1 and JX2. Instead, they are buffered through a Xilinx CoolRunner CPLD. The CoolRunner device handles 3.3V to 5V level compatibility requirements for the keyboard signals. As delivered, the CoolRunner is pre-programmed for a standard pass through connection mode.

Table 6 – Keyboard JP3 Pin Assignments

JP3 Pin #	Signal Name (at JX1/2))
1	PLD_KB_DATA
2	N/C
3	GND
4	5V
5	PLD_KB_CLK
6	N/C
7	GND
8	GND
9	GND

2.8 Optional LCD Interface

The P160 module provides a 2x7 I/O header (JP12) for an optional LCD connection (Seiko L1672 compatible with additional Samtec SSQ-107-01-F-D receptacle). The following table shows the JP12 pin assignments for the LCD connection. It should be noted that R26 potentiometer located on the I/O module is used to control the contrast of the LCD panel.

The signals present on JP12 are not driven directly from the P160 connectors JX1 and JX2. Instead, they are buffered through a Xilinx CoolRunner CPLD. The CoolRunner device handles 3.3V to 5V level compatibility requirements for the LCD. As delivered, the CoolRunner is pre-programmed for a standard pass through connection mode. Also note that the LCD data signals D0 through D7 going to the CPLDare shared with the Flash and SRAM memory.

Table 7 – JP12 LCD Connector Pin Assignments

Signal Name (at JX1/2)	JP12 Pin #		Signal Name (at JX1/2)
D7	1	2	D6
D5	3	4	D4
D3	5	6	D2
D1	7	8	D0
PLD_LCD_EN	9	10	PLD_LCD_R/Wn
PLD_LCD_RS	11	12	Contrast Voltage
GND	13	14	**+5V**

2.9 CoolRunner CPLD

A Xilinx CoolRunner CPLD is included as a buffering device between the module I/O and the LCD and keyboard connectors. In addition, there are two user I/O signals and two clock signals that connect between the JX1 connector and the CPLD. These signals are user defined and can be used as needed.

Table 8 – CoolRunner User Pin Assignments

JX1 Pin #	JX1 Signal Name	CoolRunner Pin #
A37	USERIO_1	B10
A39	USERIO_2	F10
B40	PLD_CLK0	C5
B39	PLD_CLK2	C7

2.10 P160 Communication Module Signal Assignments

The following tables show the P160 connector pin assignments to the P160 Communication Module connectors (JX1 & JX2).

Table 9 – JX1 User I/O Connector

I/O Module Usage	I/O Connector Signal Name	JX1 Pin #		I/O Connector Signal Name	I/O Module Usage
NC	NC	A1	B1	FPGA.BITSTREAM	NC
GND	**GND**	A2	B2	SM.DOUT/BUSY	NC
NC	NC	A3	B3	FPGA.CCLK	NC
Vin	**Vin**	A4	B4	DONE	NC
NC	NC	A5	B5	INITn	NC
GND	**GND**	A6	B6	PROGRAMn	NC
NC	NC	A7	B7	NC	NC
3.3V	**3.3V**	A8	B8	LIOB8	USB_VPO
USB_VM	LIOA9	A9	B9	LIOB9	USB_VMO
GND	**GND**	A10	B10	LIOB10	USB_VP
USB_OEn	LIOA11	A11	B11	LIOB11	USB_RCV
2.5V	**2.5V**	A12	B12	LIOB12	RS232_TX
ETH_MDIO	LIOA13	A13	B13	LIOB13	RS232_RX
GND	**GND**	A14	B14	LIOB14	ETH_MDC
ETH_RXD2	LIOA15	A15	B15	LIOB15	ETH_RXD3
Vin	**Vin**	A16	B16	LIOB16	ETH_RXD1
ETH_RXDV	LIOA17	A17	B17	LIOB17	ETH_RXD0
GND	**GND**	A18	B18	LIOB18	NC
ETH_TXER	LIOA19	A19	B19	LIOB19	ETH_RXER
3.3V	**3.3V**	A20	B20	LIOB20	NC
ETH_TXD0	LIOA21	A21	B21	LIOB21	ETH_TXEN
GND	**GND**	A22	B22	LIOB22	ETH_TXD1
ETH_TXD3	LIOA23	A23	B23	LIOB23	ETH_TXD2
2.5V	**2.5V**	A24	B24	LIOB24	ETH_COL
MEM.ALBn	LIOA25	A25	B25	LIOB25	ETH_CRS
GND	**GND**	A26	B26	LIOB26	MEM.BLBn
MEM.AUBn	LIOA27	A27	B27	LIOB27	MEM.BUBn
Vin	**Vin**	A28	B28	LIOB28	PLD_LCD_EN
PLD_KB_DATA	LIOA29	A29	B29	LIOB29	PLD_LCD_RS
GND	**GND**	A30	B30	LIOB30	PLD_LCD_R/WN
PLD_KB_CLK	LIOA31	A31	B31	LIOB31	PHY_RESETn
3.3V	**3.3V**	A32	B32	LIOB32	I2C_DATA
ETH_RXC	LIOA33	A33	B33	LIOB33	I2C_CLK
GND	**GND**	A34	B34	LIOB34	SPI_OUT
ETH_TXC	LIOA35	A35	B35	LIOB35	SPI_IN
2.5V	**2.5V**	A36	B36	LIOB36	SPI_CLK
USER_IO_1	LIOA37	A37	B37	LIOB37	MEM_RESETn
GND	**GND**	A38	B38	LIOB38	MEM_DU
USER_IO_2	LIOA39	A39	B39	LIOB39	PLD_CLK2
Vin	**Vin**	A40	B40	LIOB40	PLD_CLK0

Table 10 – JX2 User I/O Connector

I/O Module Usage	I/O Connector Signal Name	JX2 Pin #		I/O Connector Signal Name	I/O Module Usage
A8	RIOA1	A1	B1	**GND**	**GND**
A19	RIOA2	A2	B2	RIOB2	A11
A9	RIOA3	A3	B3	**Vin**	**Vin**
A12	RIOA4	A4	B4	RIOB4	A15
A13	RIOA5	A5	B5	**GND**	**GND**
A21	RIOA6	A6	B6	RIOB6	A10
A22	RIOA7	A7	B7	**3.3V**	**3.3V**
A14	RIOA8	A8	B8	RIOB8	A16
D6	RIOA9	A9	B9	**GND**	**GND**
D15	RIOA10	A10	B10	RIOB10	D13
D7	RIOA11	A11	B11	**2.5V**	**2.5V**
D12	RIOA12	A12	B12	RIOB12	D14
D4	RIOA13	A13	B13	**GND**	**GND**
D5	RIOA14	A14	B14	RIOB14	D3
D11	RIOA15	A15	B15	**Vin**	**Vin**
D9	RIOA16	A16	B16	RIOB16	D10
D2	RIOA17	A17	B17	**GND**	**GND**
D0	RIOA18	A18	B18	RIOB18	D8
MEM.OEn	RIOA19	A19	B19	**3.3V**	**3.3V**
MEM.CE1Sn	RIOA20	A20	B20	RIOB20	MEM.CEFn
D1	RIOA21	A21	B21	**GND**	**GND**
D22	RIOA22	A22	B22	RIOB22	D31
D23	RIOA23	A23	B23	**2.5V**	**2.5V**
D29	RIOA24	A24	B24	RIOB24	D30
D28	RIOA25	A25	B25	**GND**	**GND**
D21	RIOA26	A26	B26	RIOB26	D20
D19	RIOA27	A27	B27	**Vin**	**Vin**
D27	RIOA28	A28	B28	RIOB28	D18
D26	RIOA29	A29	B29	**GND**	**GND**
D24	RIOA30	A30	B30	RIOB30	D16
D25	RIOA31	A31	B31	**3.3V**	**3.3V**
D17	RIOA32	A32	B32	RIOB32	A0
A4	RIOA33	A33	B33	**GND**	**GND**
A1	RIOA34	A34	B34	RIOB34	A17
A2	RIOA35	A35	B35	**2.5V**	**2.5V**
A5	RIOA36	A36	B36	RIOB36	A3
A6	RIOA37	A37	B37	**GND**	**GND**
A7	RIOA38	A38	B38	RIOB38	A18
MEM.RY/BY	RIOA39	A39	B39	**Vin**	**Vin**
MEM.WEn	RIOA40	A40	B40	RIOB40	A20

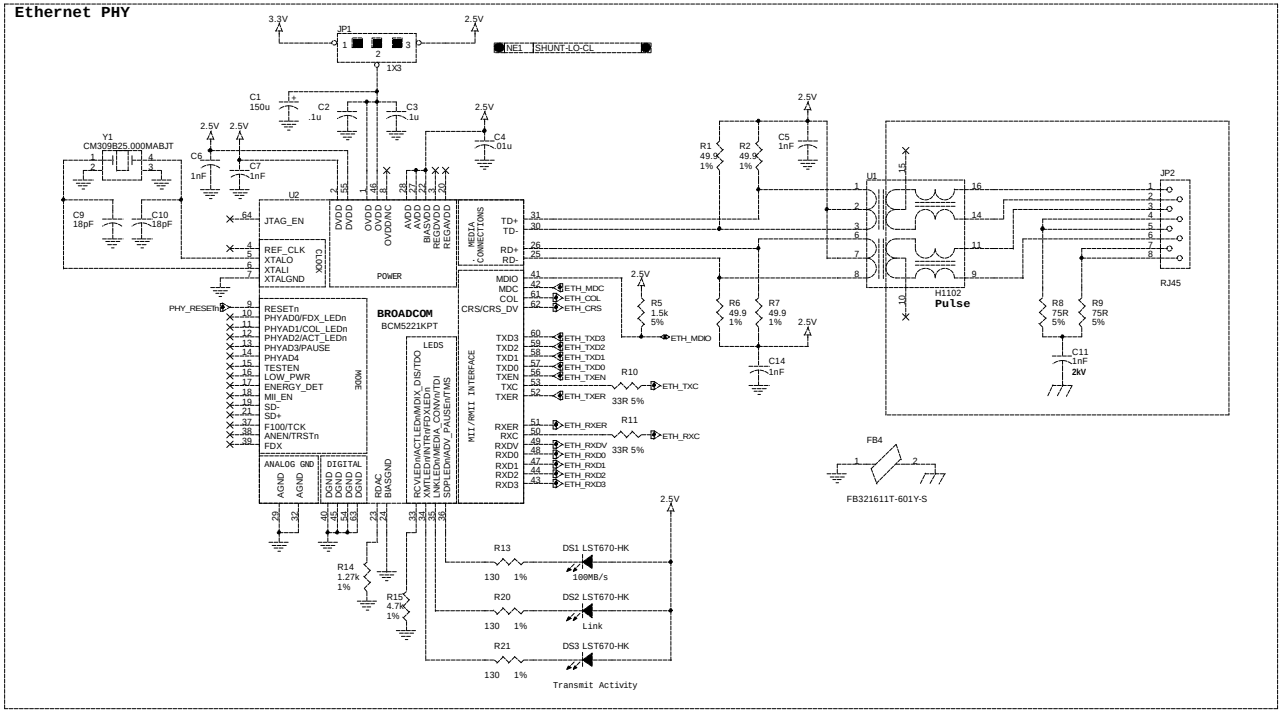
Revision History

V1.0	**Initial Release**	**2/13/02**
V2.0	**Rev 2 Board Release** Added Table 1 – Ethernet pin assignments Added Table 2 – RS232 pin assignments Added Table 5 – Flash/SRAM pin assignments Removed User I/O 3 from Table 8 Removed JTAG signals from JX1 in Table 9	**12/1/02**

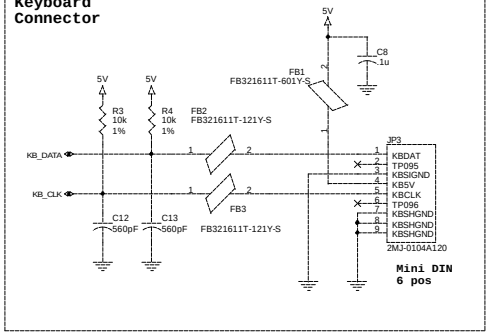
Appendix A

P160 Communication Module (Rev 2) Schematics

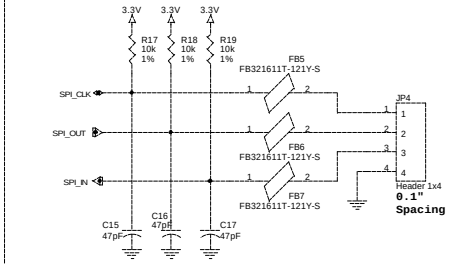
Ethernet PHY



PS/2 Keyboard Connector



Serial Peripheral Interface (SPI)



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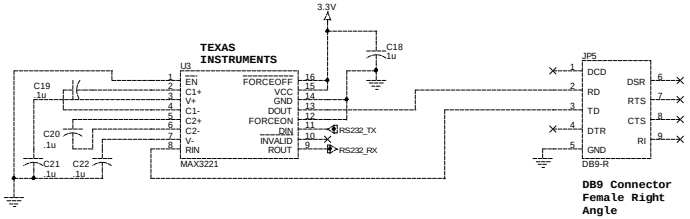

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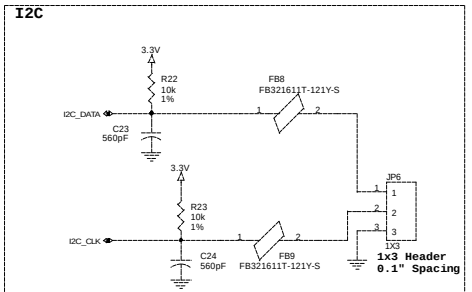

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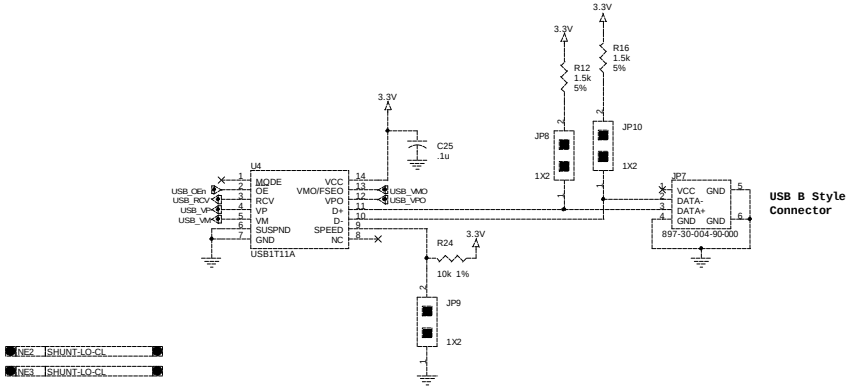

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External Interfaces

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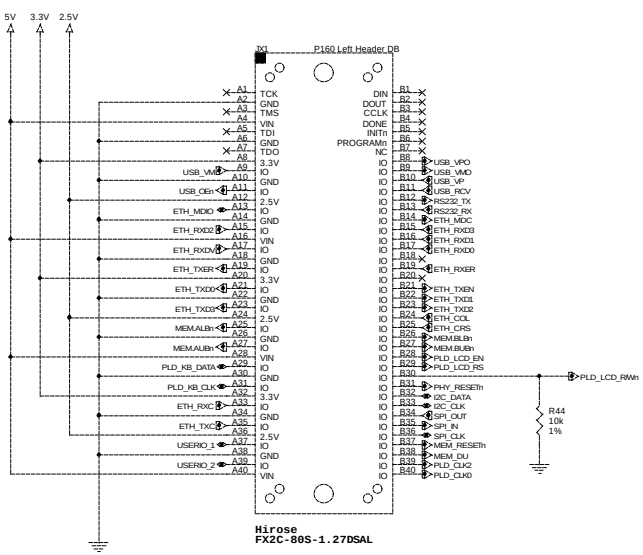
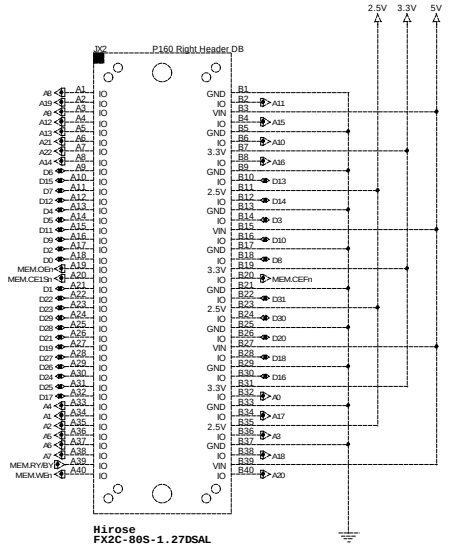
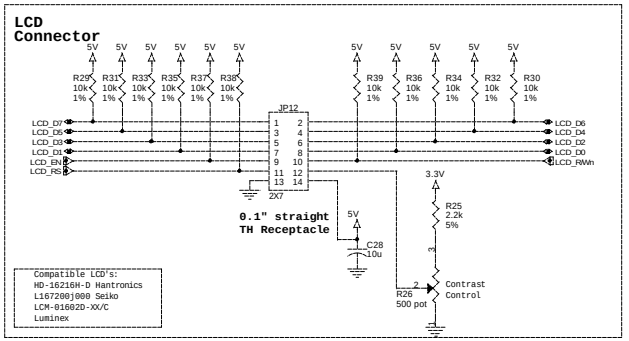
Designer	Sheet
Brian Dewald	1 of 3







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Motherboard Connectors, LCD Connector & 5V Regulator

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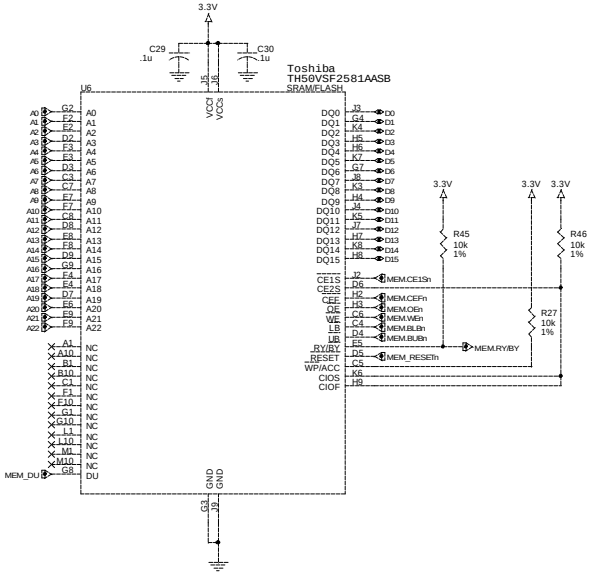

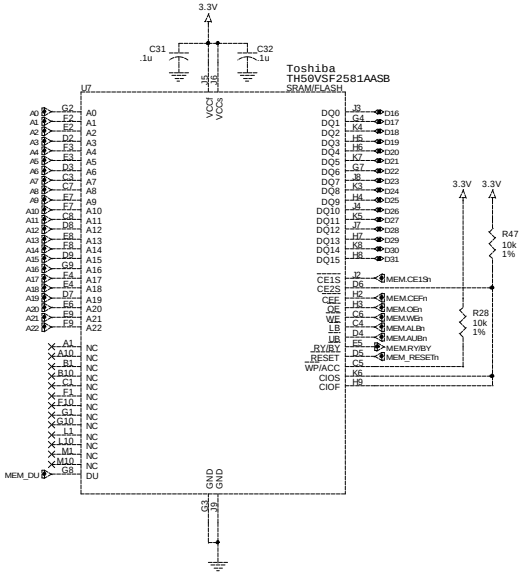

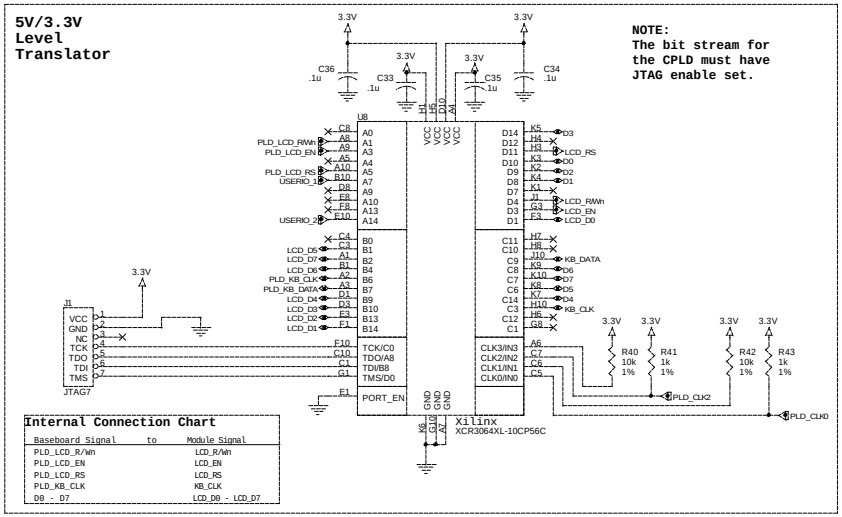

MicroBlaze Communications Board DS-BD-MBEXP1

Memory & CPLD Level Translator

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C	2
Designer	Sheet
Brian Dewald	3 of 3