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Interfacing LVPECL 3.3V Drivers With Xilinx 2.5V Differential Receivers

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Summary

This application note describes how to interface 3.3V differential LVPECL drivers (Low-Voltage Positive Emitter Coupled Logic) with Xilinx 2.5V differential receivers, including Virtex-II Pro™/Virtex-II Pro™ X 2.5V LVPECL/LVDS and Spartan®-3 2.5V LVDS. Several interface modifications are presented with supporting IBIS simulation results. By reducing the 3.3V LVPECL common mode voltage, you can safely interface to 2.5V LVPECL and LVDS receivers in Virtex-II Pro/Virtex-II Pro X and Spartan-3 (and future Xilinx devices that support 2.5V differential inputs).

Introduction

Differential 3.3V LVPECL is commonly used for the transmission of high speed, low-jitter clocks and high bit rate data. LVPECL offers the advantage of high noise immunity over relatively long interconnects. Virtex-E and Virtex-II LVPECL-configured differential input buffers can be directly connected to non-Xilinx 3.3V LVPECL drivers. However, Virtex-II Pro and Spartan-3 differential receivers cannot directly receive 3.3V LVPECL output levels with standard receiver termination.

Virtex-II Pro, Virtex-II Pro X, and Spartan-3 Differential 2.5V Input Specification

A standard 2.5V LVPECL interface is shown in Figure 1. The recommended termination technique for interfacing Xilinx differential receivers to 2.5V differential standards is a parallel 100 Ohm termination between the receiver inputs (as shown in Figure 1). The acceptable input level range for Virtex-II Pro, Virtex-II Pro X, and Spartan-3 differential input receivers is summarized in Table 1. An IBIS simulation of the interface is shown in Figure 2. The driver and receiver used in the simulation were Virtex-II Pro 2.5V LVPECL and the receiver voltages were probed at the die pads (see Figure 2 for simulation results).

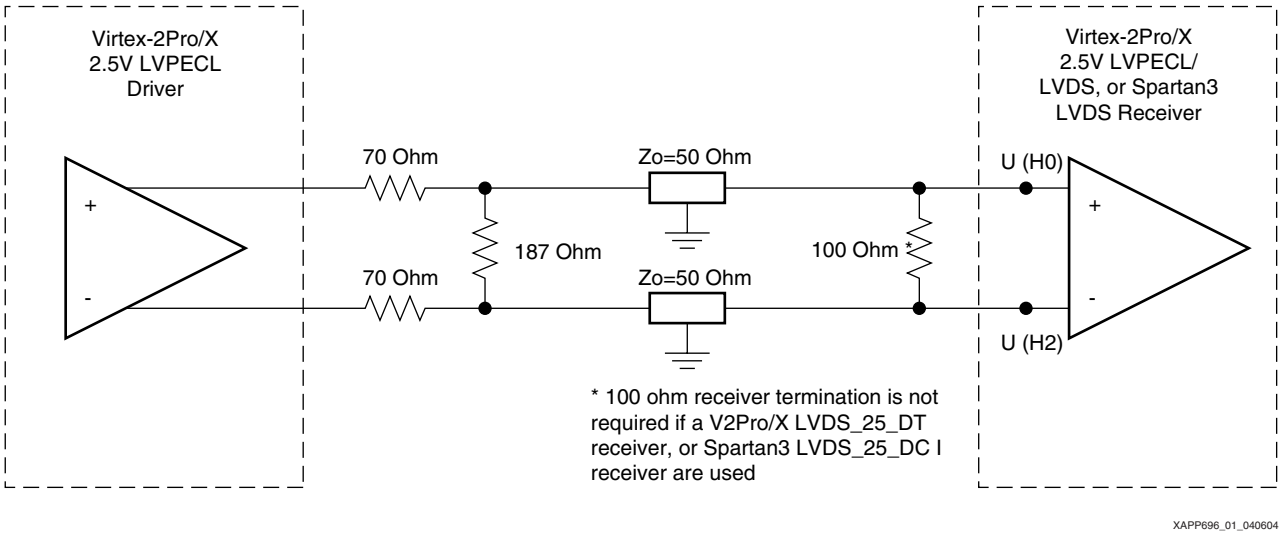

Figure 1: **Virtex-II Pro/Virtex-II Pro X 2.5V LVPECL Termination Circuit**

Table 1: **Xilinx Virtex-II Pro/Virtex-II Pro X and Spartan-3 Differential Receiver DC Levels**

DC Parameter	Symbol	Condition	Min	Typ	Max
Differential Input Voltage (data sheet specification)	V_{IDIFF}	Vcm=1.25V	0.1V		1 V
Input Common-Mode Voltage (data sheet specification)	V_{ICM}	V_{IDIFF}=+-350mV	0.3V		2.2V
Simulated Differential Input Voltage	$V_{IDIFFSIM}$	Measured from Figure 2		0.82V	
Simulated Common-mode Input Voltage	V_{ICMSIM}	Measured from Figure 2		1.2V	

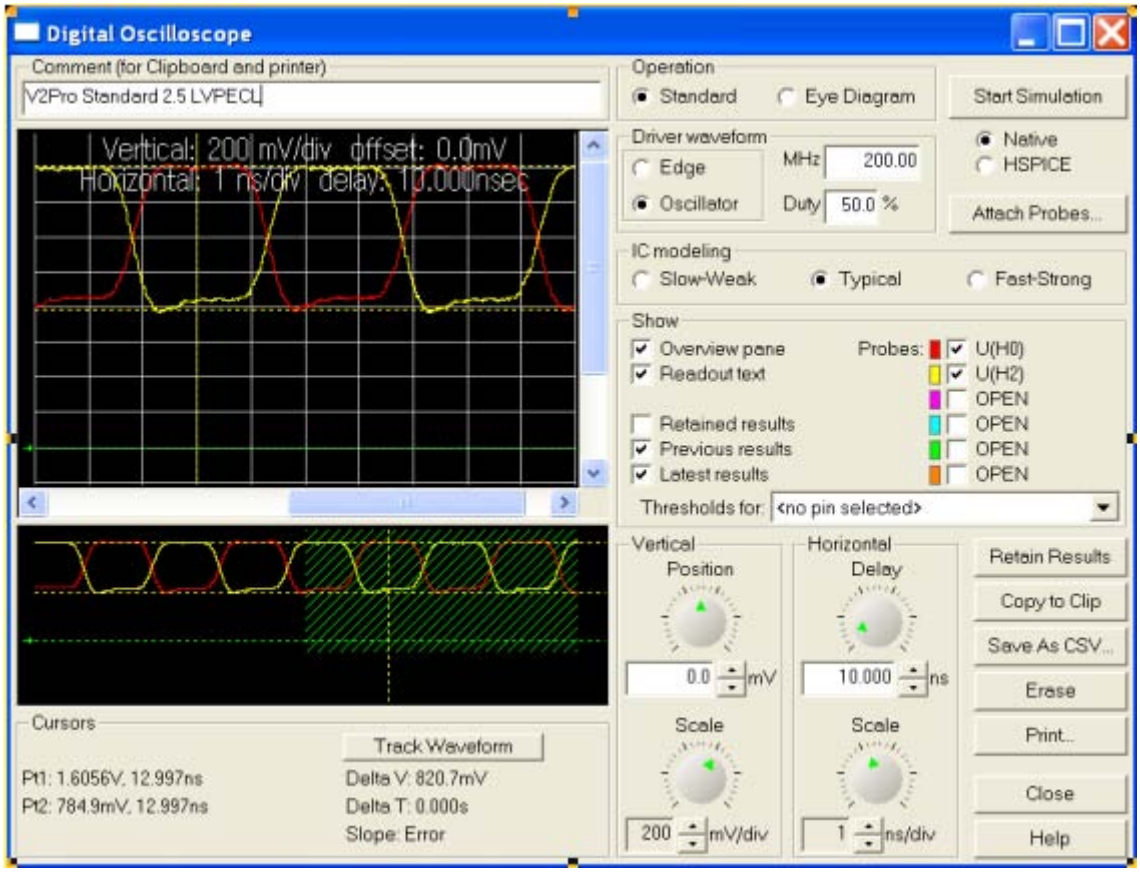

Figure 2: **Virtex-II Pro 2.5V LVPECL Receiver Voltage Levels**

3.3V LVPECL Output Specification

Many parts used in high speed transceiver designs use 3.3V LVPECL differential standard I/O. The 3.3V LVPECL output voltage levels vary from vendor to vendor. However, a maximum output level exceeding 2.5V is commonly specified in vendor data sheets. A common termination technique used for 3.3V LVPECL interfaces is shown in Figure 3.

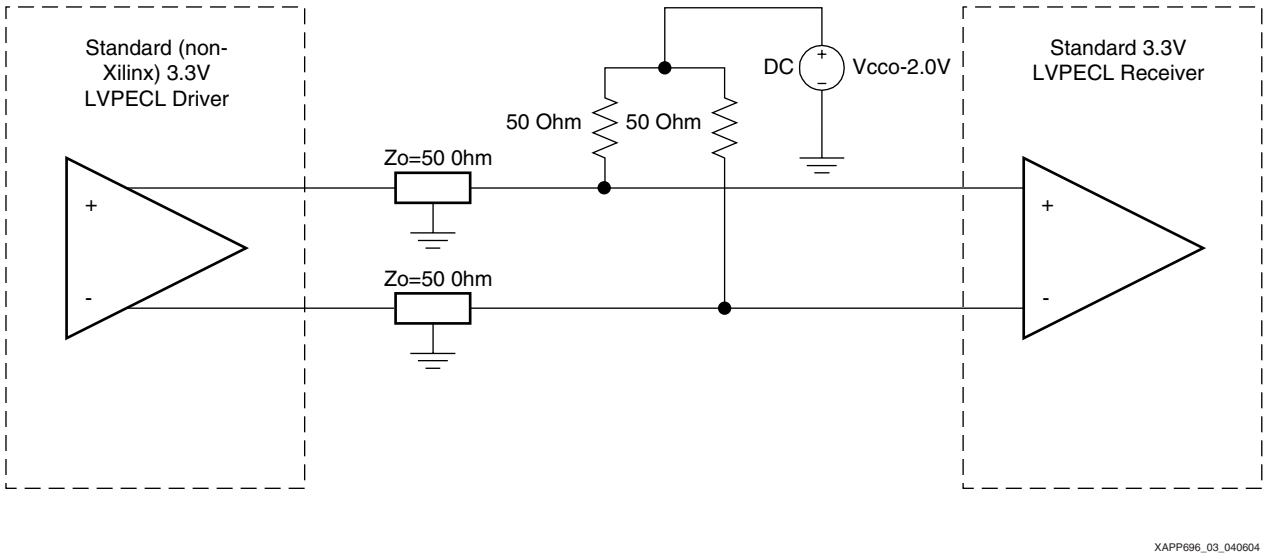

Figure 3: **Standard 3.3V LVPECL Termination**

Interface Modification Advice

When interfacing a 3.3V LVPECL driver to a Xilinx Virtex-II Pro, Virtex-II Pro X, or Spartan-3 2.5V differential receiver, you should first consider the output specification for the driver. If the output levels of the driver are within the Xilinx specified receiver levels, then you can use standard receiver termination. This typically consists of a 100 Ohm parallel termination, or 50 Ohm split termination to Vcco-2.0V.

For driver output levels that exceed the specified receiver input levels, you can use custom termination techniques to reduce the common mode voltage level or the voltage swing.

DC Coupled Receiver Common Mode Voltage Shift

By replacing the standard receiver termination with a custom termination network, you can reduce the common mode voltage while maintaining an optimal voltage swing. An example of such a technique is shown in Figure 4. Six termination resistors are required for each differential receiver.

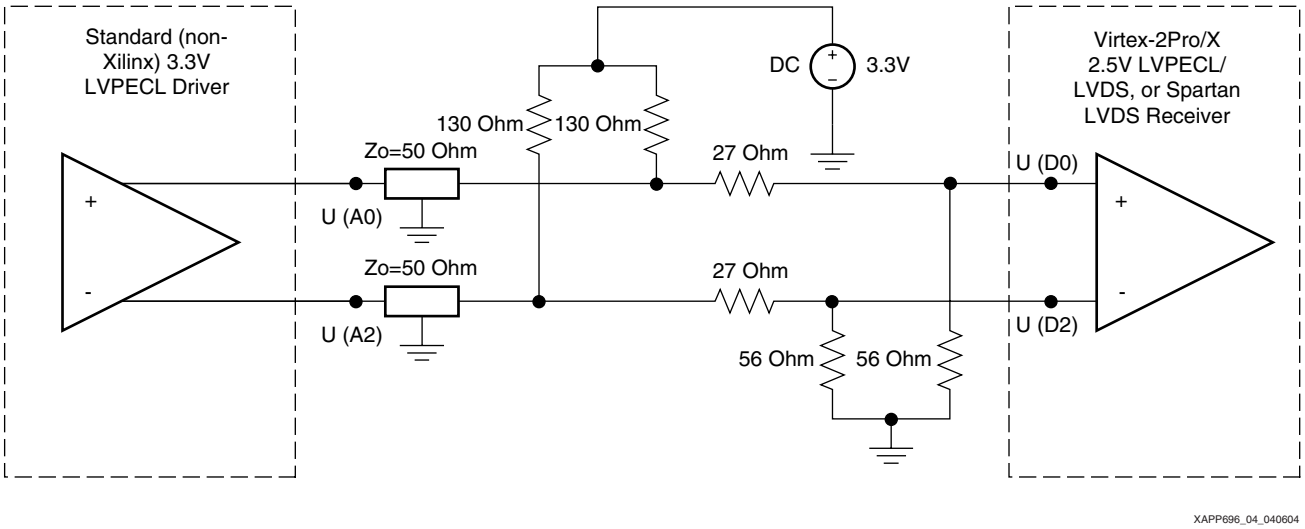

Figure 4: **3.3V LVPECL to 2.5V Differential Receiver DC Coupled Interface**

The circuit shown in Figure 4 was simulated in IBIS. In the results in Figure 5, the common mode voltage was reduced from approximately 2.25 V (at the driver output) to 1.5 V (at the receiver input), comfortably meeting the Xilinx Virtex-II Pro, Virtex-II Pro X, and Spartan-3 differential receiver input specifications. The simulation results are summarized in Table 2.

Table 2: **Summary of Figure 5 IBIS Simulation Results**

Parameter	Symbol	Typical
Simulated Differential output voltage	Vodiffsim	0.7V
Simulated Output common-mode voltage	Vocmsim	2.25V
Simulated Differential input voltage	Vidiffsim	0.5V
Simulated Input common-mode voltage	Vicmsim	1.5V

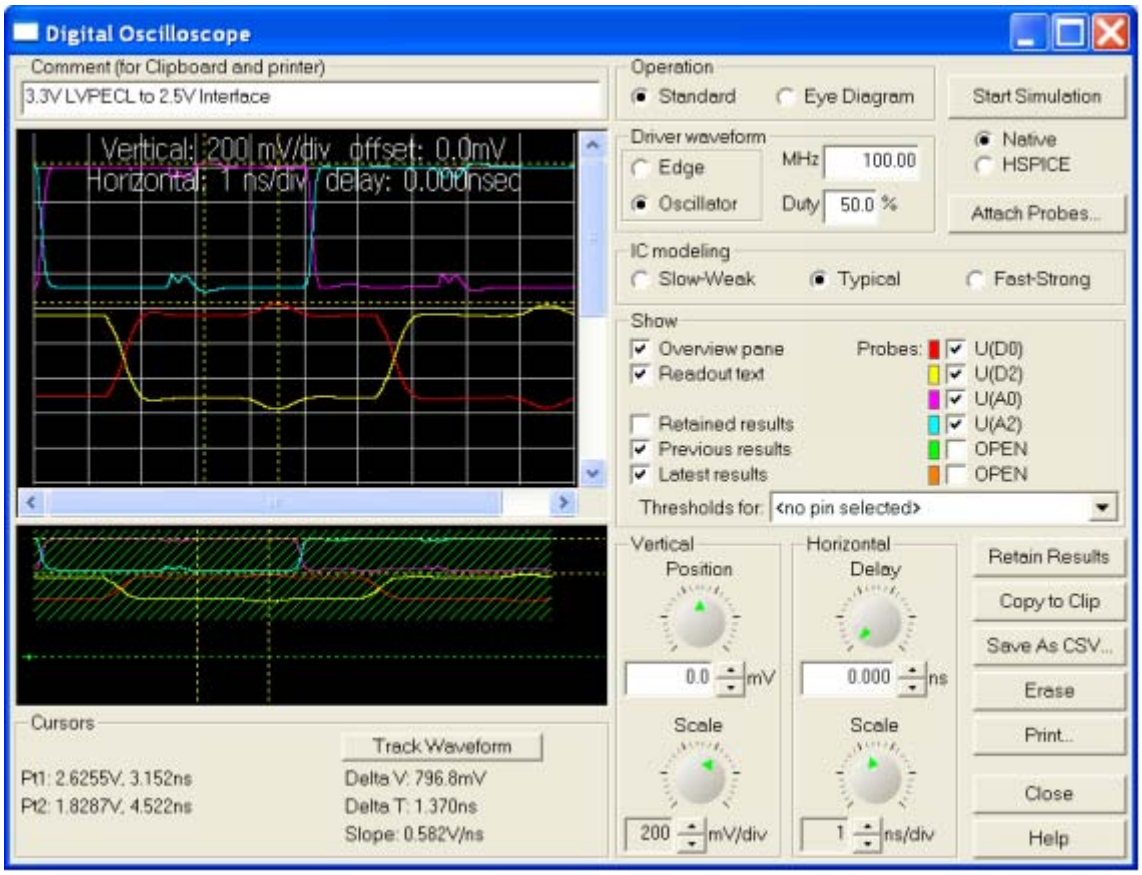

Figure 5: **3.3V LVPECL to 2.5V Receiver IBIS Simulation**

Note: The termination network shown in Figure 4 is intended for reference purposes only.

The optimal termination values are dependent on the driver output levels and might need to be adjusted to achieve optimal voltage levels at the receiver.

AC Coupled Receiver Common Mode Voltage Shift

Inserting a series capacitor and biasing network into each leg of the differential receiver allows a reduction of the common mode voltage. This technique can provide protection against extreme DC voltages and can be useful for board-to-board or system-to-system interfaces. An example of such an interface is shown in Figure 6. AC coupling of links that have long idle periods, or where the signal is not DC balanced (the number of 1s and 0s average over time is not equal) might not be suitable. Also, the low frequency cut-off point of the high-pass filter formed by the series capacitor and receiver termination must be significantly lower than the minimum spectral frequency content, or data loss can occur. The component values shown in Figure 6 are suitable in applications where the minimum significant spectral content is about 1 MHz.

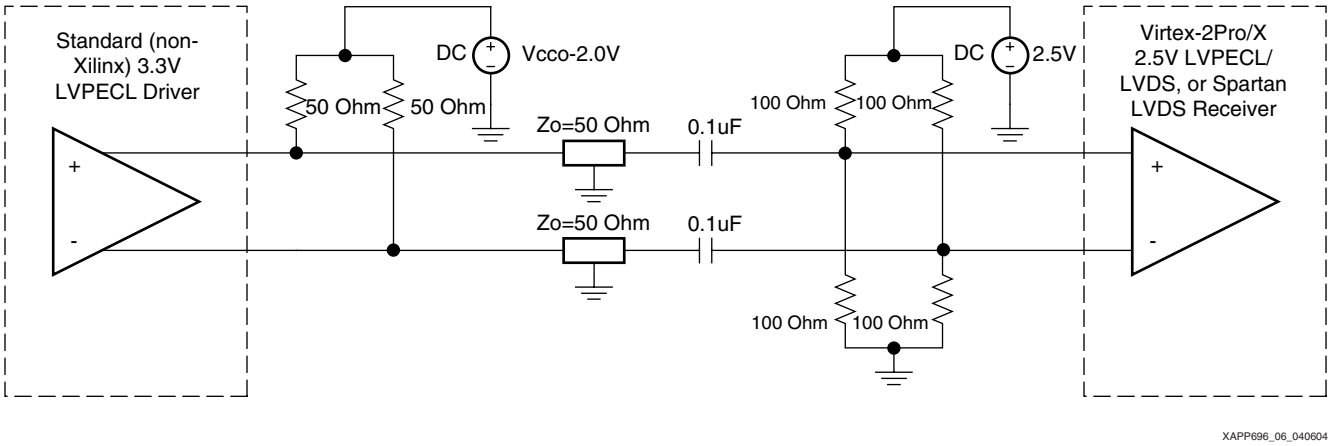

Figure 6: **3.3V LVPECL to 2.5V Differential Receiver AC Coupled Interface**

Driver Vcco Reduction

You can also reduce the common mode output voltage to a low enough level by reducing the driver Vcco value. You can evaluate this option by running an IBIS or SPICE simulation, or by bench testing.

Conclusion

Virtex-II Pro and Spartan-3 typically cannot directly receive LVPECL 3.3V levels using standard 100 Ohm parallel receiver termination. However, by utilizing custom AC or DC coupled termination schemes, you can effectively implement such an interface. The LVPECL driver output voltage device specification should always be considered and IBIS or SPICE simulation should be performed to determine the optimal interface termination scheme.

Revision History

The following table shows the revision history of this document.

Date	Version	Revision
05/21/04	1.0	Initial Xilinx release.