Realization and electrical characterization of ultrathin crystals of layered transition-metal dichalcogenides

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Ultrathin crystals of the layered transition-metal dichalcogenide MoS_2 (semiconducting) and TaS_2 (metallic) were obtained by mechanical peeling or chemical exfoliation techniques and electrically contacted using electron-beam lithography. The MoS_2 devices showed high field-effect mobility in the tens of $cm^2/V\,s$ and an on/off ratio higher than 10^5. The TaS_2 devices remained metallic despite the fabrication process and showed an enhancement of the superconducting transition temperature and disappearance of the charge density wave phase anomaly at low temperature. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2407388]

I. INTRODUCTION

The electronic industry needs high quality, flexible, and consequently thin semiconductor materials in order to realize devices in situations where standard silicon chips cannot work due to expense and geometry. So far research has focused on organic materials[1,2] because of their potentially low cost. But their poor mobility has prompted several groups to look for inorganic alternatives.[3,4] Semiconducting layered transition-metal dichalcogenide (LTMD) compounds, consisting of subnanometer-thick layers bound to each other by weak van der Waals forces, are promising candidates for thin-film transistors (TFTs); single-crystal WSe_2 has been shown to have hole mobility up to 500 $cm^2/V\,s$ in single crystals[5] (comparable to Si) and thin films of $SnS_{2-2x}Se_x$ have mobilities exceeding 10 $cm^2/V\,s$, significantly higher than the best organic semiconductors.[2]

Moreover, thin LTMDs are promising materials for nanoscience research. Recently there has been significant renewed interest in self-assembled two-dimensional materials, such as graphene and LTMDs, prepared in two-dimensional form.[6–8] LTMDs are particularly interesting in this context; they have a rich variety of electronic states [metallic, semiconductor, superconductor, and charge density waves (CDWs)] that have fascinated basic researchers for several years. Furthermore, thin LTMDs could provide a route to realizing nanometer-thickness metallic contacts to other nanodevices (such as single molecules), which would allow visualization by scanning-probe techniques.

In early experiments on thin LTMD compounds prepared by exfoliation,[9–12] indirect measurements indicated the presence of isolated monolayers or of some samples with an area constituted of a single layer. However, the samples were too small to carry out electron transport measurements on isolated, uniform, and thin devices. More recently, the preparation of single atomic layers of MoS_2 and $NbSe_2$ by mechanical cleaving has been reported, with some limited electron transport data;[6] both MoS_2 (semiconducting) and $NbSe_2$ (nominally metallic) showed field-effect mobilities in the range of 0.5–3 $cm^2/V\,s$ and poor on-off ratios (<10). No low temperature measurements were reported.

In this paper, we report the fabrication by two different techniques of ultrathin films made of few layers (that we term nanopatches) of $2H-TaS_2$, a metallic LTMD, and MoS_2, a semiconductor LTMD. We used microfabrication tools to make nanodevices out of these nanopatches in order to perform electron transport measurements. MoS_2 nanopatches are semiconducting, with mobilities in the tens of $cm^2/V\,s$, and on-off ratios exceeding 10^5. The poor subthreshold slope and activated conductance with a gate-voltage-dependent activation energy indicate a high density of charge-trap states in MoS_2 nanopatch transistors, similar to organic TFTs. TaS_2 nanopatches are metallic for samples as thin as 8 nm. TaS_2 nanopatches show no CDW anomaly in the temperature-dependent resistivity and an enhancement of the superconducting transition temperature.

Bulk $2H-MoS_2$ is (in general) a *n*-type semiconductor and is resistant to oxidation. It is used as a solid lubricant or a catalyst in industry. It has an indirect band gap on the order of 1 eV,[13] which has been reported to be as small as 0.2 eV in thin films.[14] The thickness of one layer is equal to 6.15 Å. The in-plane resistivity is about 10 Ω cm and the interlayer resistivity is 200 times larger. Bulk $2H-TaS_2$ is metallic at room temperature, undergoes a charge density wave phase transition at $T=70$ K,[15,16] and superconducts below 0.8 K.[15] The thickness of one layer is equal to 6.04 Å. The in-plane resistivity at room temperature is about 10^{-4} Ω cm.[15]

II. EXPERIMENT

A. Preparation of MoS_2 nanopatches

The MoS_2 sample (SPI Supplies) we have used is obtained from geological material that has been extracted in Otter Lake, Ontario, Canada and consists of one big crystal of a cubic centimeter. The thinning procedure is close to the technique to get clean surfaces of highly oriented pyrolytic

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graphite (HOPG) or mica and consists of peeling layers of the crystal using tape (3M Scotch brand). First, the LTMD crystal is placed on the sticky side of a piece of tape so that the basal plane of the crystal is parallel to the plane of the tape. The sticky side of another piece of tape is placed on top of the opposite side of the crystal to form a sandwich made of tape/LTMD/tape. Then the two pieces of tape are pulled apart. As the force between the layers of the crystal is weaker than the adhesion force between the crystal and the tape, the crystal splits into two crystals of same surface areas but smaller thicknesses. This process is repeated several times until the crystal is barely visible to the eyes on the tape. The next step consists of sticking the tape to a Si chip (degenerately doped Si with 500 nm SiO_2 which will later function as a gate dielectric) and dipping this chip in a solution of ethylbutyl acetate for an hour. This solvent can partially solubilize the adhesive of the tape and so help to separate the crystal and the tape. After separation some pieces of crystal remain on the chip. The remaining pieces of crystal on the tape are removed with tweezers and transferred to a different chip in solution. Then both chips are blown dry with nitrogen. If necessary the crystals on the chips are further thinned using tape. The use of tape leaves some residue on the substrate but most of the time it may be removed simply by cleaning with isopropanol.

B. Preparation of TaS_2 nanopatches

We followed a well established recipe to grow TaS_2 crystals[17] by vapor transport in a quartz tube. We used sulfur (99.999% pure, Alfa Aesar) and tantalum (99.9% pure, Alfa Aesar) as starting materials and iodine (99.999% pure, Cerac) as a vapor transport agent. The typical size of the crystals was 1 $mm^2 \times 10$ μm.

The thinning procedure is based on the intercalation of a reactive component (such as lithium) inside the crystal. The TaS_2 crystals were exposed to *n*-butyl lithium in a dry box environment. The crystals were removed from the dry box in a sealed container which was opened under water. The intercalated Li reacts with water to produce hydrogen that expands and tends to separate the layers of the crystal (see Ref. 12 for details), resulting in a suspension of nanopatches. The thicker nanopatches gradually sink to the bottom over time leaving the thinner in the top half of the solution. The nanopatches can be deposited on a surface by placing a drop of the suspension on a SiO_2 chip or the chip can be dipped into the first half of the solution and removed. The chips are cleaned in a piranha solution prior to nanopatch deposition. The nanopatches will adhere to the SiO_2 due to van der Waals forces after a few seconds. Then the water is blown dry and the nanopatches remain immobilized on the surface.

We note that while the methods employed here to fabricate thin crystals of LTMD on insulator are crude and probably unsuitable for mass production, it is not unreasonable to expect that techniques for fabricating large area LTMD devices could be developed. The "smart-cut" method[18] for producing silicon-on-insulator wafers is analogous to our mechanical exfoliation process, and techniques such as van der Waals epitaxy[19] or simple solution deposition of exfoliated material as a thick film may be able to produce large-area polycrystalline LTMD films suitable for flexible electronic devices.

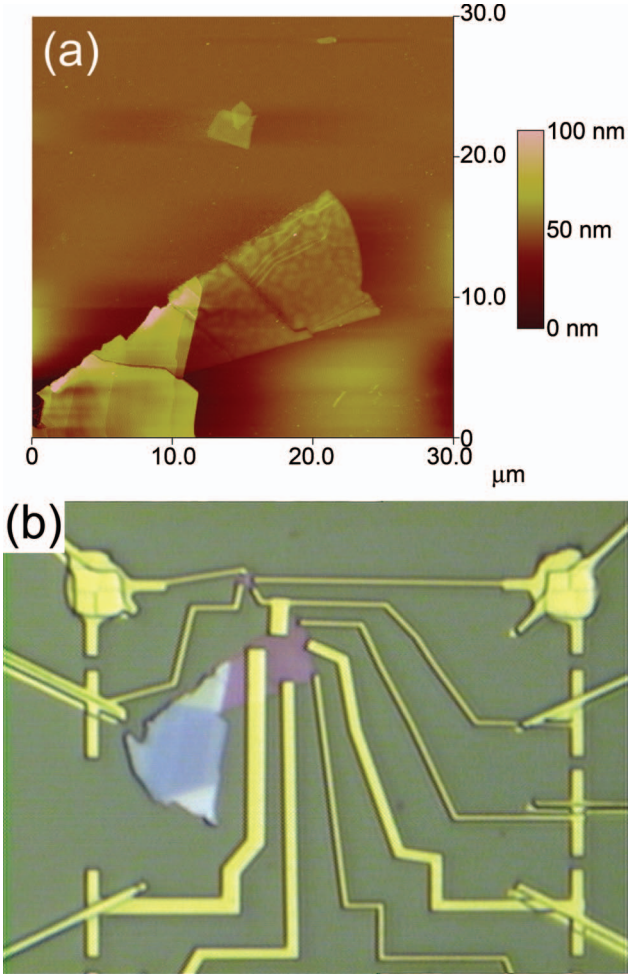

FIG. 1. (Color) (a) Atomic force microscopy image of several MoS_2 nanopatches (from 10 to 40 nm in thickness). (b) Optical images after electrical contact of the same crystals in (a). The blue and purple areas are the MoS_2 nanopatches, the yellow features are Cr/Au leads defined by lithography, and the green background is the SiO_2/Si substrate.

C. Realization of devices

Once on the SiO_2/Si chip, nanopatches are optically visible for thickness t greater than ~4 nm. They look metallic for $t > 40$ nm and are transparent but of different colors than the substrate for $t < 40$ nm. Hence the bare location of a crystal on the chip can be first determined with an optical microscope. Then an alignment marker array close to this location is lithographically patterned. With the help of an atomic force microscope (AFM), a scanning electron microscope (SEM), or an optical microscope, the entire marker array can be mapped in order to determine the exact position of the nanopatch relative to the markers. AFM and SEM are more sensitive than optical microscope, so we sometimes find during this part of the process nanopatches with $t < 4$ nm. Finally, electrical contacts are fabricated by electron-beam lithography and evaporating 2.5 nm of Cr and 100 nm of Au (see Fig. 1).

The main difference of this process compared to the previous studies on LTMD thin films[9–12] is that we can measure directly the thickness by AFM of the crystal we are going to measure. We select the crystals that are as perfect as possible with uniform thickness (same number of layers across the entire sample), little mechanical damage, and the smallest thickness possible.

III. RESULTS AND DISCUSSION

A. TaS_2 nanopatches

We have obtained nanopatches of TaS_2 as thin as $t=2$ nm [~3 ML (monolayer)] but were unable to observe conduction in nanopatches with $t<8$ nm (~13 ML). The TaS_2 nanopatches have a very good aspect ratio, typically 10 nm thick and 10 μm wide. We also find that the lifetime of electronic devices is short (< one week). We suspect that the lithium hydroxide formed during the exfoliation reaction corrupts the sample; this may also explain the lack of conduction observed in the thinnest samples.

The transport measurements were carried out by applying a dc source-drain and gate voltage with a computer-controlled data-acquisition board and measuring the current through a transimpedance amplifier (DL Instruments model 1211). For the four-probe configuration, the voltage was measured by a nanovoltmeter (Keithley Instruments model 2182). The low temperature measurements were carried out in a ^{4}He gas-flow cryostat.

We have performed two-probe measurements, and four-probe measurements when possible, on seven TaS_2 devices at room temperature. The in-plane resistivity ranges from 10^{-4} Ω cm (in very good agreement with the bulk value) to 10^{-2} Ω cm for the thinnest nanopatches ($t=8$ nm). Figure 2(a) shows the four-probe resistivity versus temperature for the thinnest ($t=8$ nm) sample. The resistivity decreases linearly with temperature as expected for a metallic material. This indicates that the sample is probably still in the $2H$ coordination mode and did not switch to the metastable $1T$ mode during the exfoliation process.[20]

At low temperature the device does not show the CDW anomaly at 70 K (Refs. 15 and 16) but has a higher superconducting transition temperature than the bulk value of 0.8 K [see Fig. 2(b)]. Similar behavior has already been seen in Ref. 15 for intercalated TaS_2 crystals and for pristine TaS_2 with interlayer disorder. (Note that in $NbSe_2$, where the CDW has a smaller effect on superconductivity,[21] the superconducting transition temperature decreases with layer thickness below about six layers.[11]) So we conclude that this is not related to any size effect but instead due to reduced interlayer interaction due to the intercalation/exfoliation process. This indicates that the lattice parameter in the perpendicular direction may be larger than the bulk one and that our estimate of the number of layers is only an upper bound.

The superconducting transition is not very abrupt with temperature and spans from 4 K (onset of resistance drop) to 2 K (zero resistance); we attribute the wide transition to inhomogeneities in the crystal. The multiple onsets in the IV curve at 1.5 K in Fig. 2(b) support this hypothesis and indicate that some layers or some part of the nanopatch has a different critical current. The lowest critical current is 160 nA, which corresponds to a rather low current density about 100 A/cm^2. Although the nanopatches seem slightly disordered, we saw no evidence of weak localization and the carrier density is high enough so that we observed no dependence of the conductance on gate voltage up to +/−100 V (applied to the Si substrate) at any temperature.

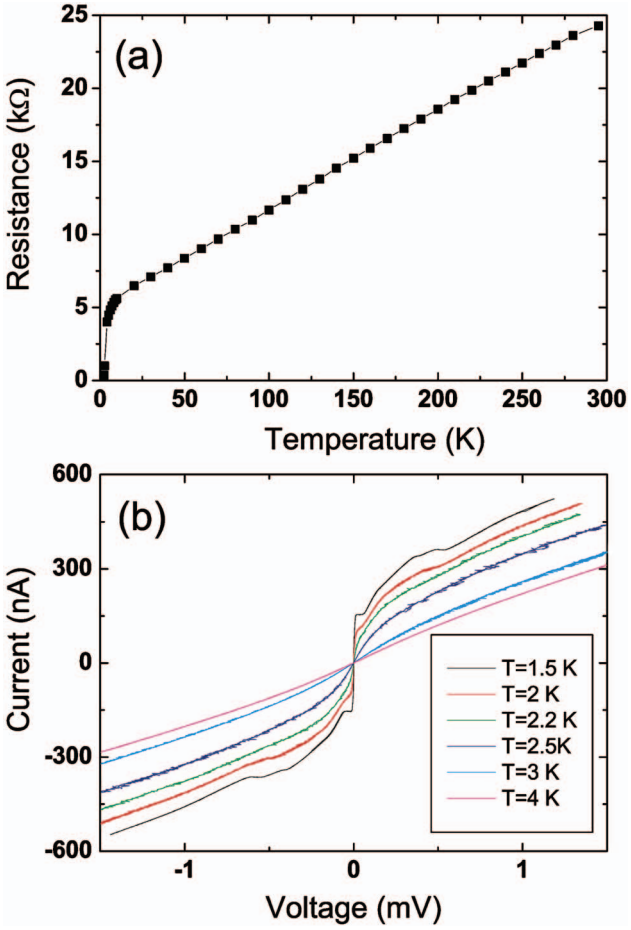

FIG. 2. (Color) (a) In-plane resistivity vs temperature of an 8-nm-thick TaS_2 nanopatch. (b) Low temperature current-voltage curves for the same crystal.

B. MoS_2 nanopatches

We have performed two-probe measurements, and four-probe measurements when possible, on ten devices at room temperature. Their thicknesses span between 8 and 40 nm and they all show comparable behaviors. The contact resistance is of the same order as the sample resistance except at low temperature where the contact starts to dominate. Although an accurate value for the in-plane resistivity is difficult to determine because the size of the contacts (2 μm wide) is comparable to the size of the sample, we estimate the in-plane resistivity at zero gate voltage and room temperature to range from 0.3 to 4 Ω cm, comparable to the bulk value of 10 Ω cm. The variation from sample to sample appears to be due to differences in threshold voltage rather than mobility. All the devices show a n-type behavior and no hole conduction has been observed for gate voltages greater than −50 V. The field-effect mobility in the four-probe configuration, defined as $\mu=(L/C_{ox}W)dG/dV_g$ (where

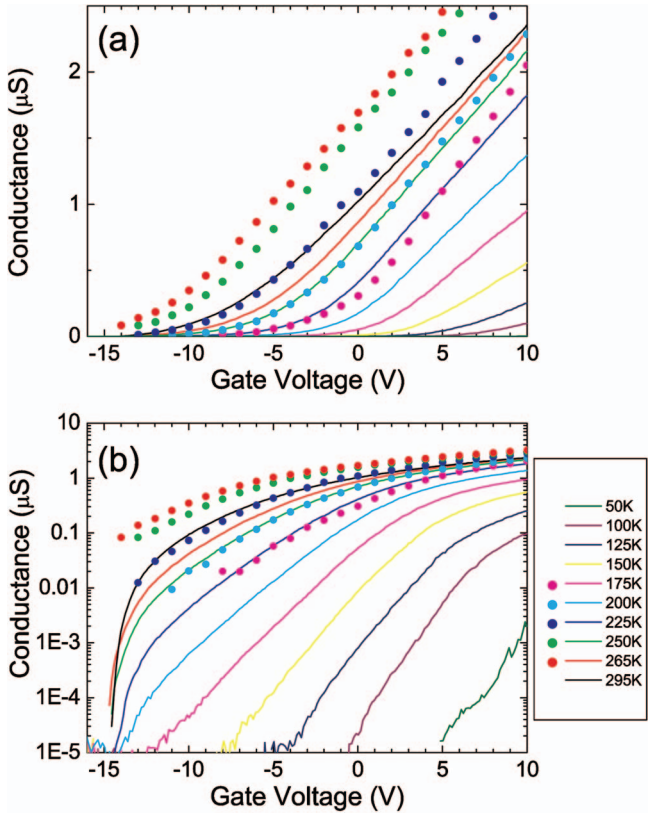

FIG. 3. (Color) Two-probe conductance (solid lines) vs gate voltage at various temperatures from 50 to 295 K for a MoS_2 field-effect transistor fabricated from an 35-nm-thick nanopatch contacted by Cr/Au electrodes on (a) linear and (b) semilogarithmic scales. Source-drain voltage is 20 mV. The four-probe conductance data for temperatures of 175 to 265 K are also plotted as solid symbols.

$C_{ox}=\varepsilon_{ox}/d_{ox}$ is the oxide capacitance per unit area with ε_{ox} the permittivity of the oxide and d_{ox} the thickness of the oxide, L the length of the device between voltage probes, W the width of the device, $G=I/V$ the conductance of the device with I the source-drain current and V the voltage between voltage probes, V_{th} the threshold voltage, and V_g the gate voltage), ranges from 10 to 50 $cm^2/V\,s$ for all the devices, though uncertainties caused by the geometry of the samples could result in errors as large as a factor of 2 in calculating the mobility. These reasonable values for the resistivity and mobility indicate that the samples are not damaged by the fabrication process. The two-probe on/off ratio is higher than 10^5 and thus suitable for applications [Fig. 3(b)].

Figure 3 shows the two-probe and four-probe conductances of a 35-nm-thick MoS_2 nanopatch with $L=4.7\ \mu m$ and $W=2.2\ \mu m$ at various temperatures. The room-temperature resistivity for this sample is 0.7 Ω cm, and the room-temperature four-probe field-effect mobility is 40 $cm^2/V\,s$, both at zero gate voltage. The subthreshold swing S, defined by $dV_g/d(\log G)$ exceeds 1 V/decade at room temperature, far from the minimum value of $kT(\log 10)/q \approx 60$ mV/decade for the ideal metal-oxide-semiconductor field-effect transistor (MOSFET), where q is the electron charge, T the temperature, and k the Boltzmann constant. Such a high value of S indicates that the oxide capacitance per unit area $C_{ox}=7\times10^{-9}\ F/cm^2$ is competing with other capacitances that are at least ten times larger.

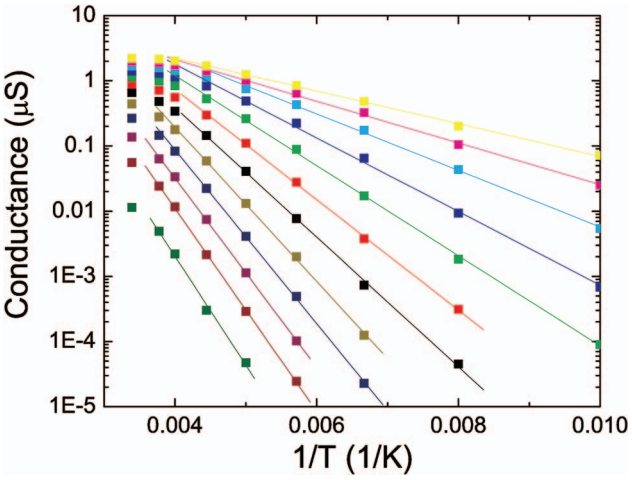

FIG. 4. (Color) Arrhenius plot of the two-probe conductance data from Fig. 3 at gate voltages from −13 to+9 V in steps of 2 V.

Typically, the most common parasitic capacitances are the depletion capacitance and the trap charge capacitance. However, the depletion capacitance cannot be an appreciable fraction of the total capacitance, since the sample thickness $t=8-40$ nm is much smaller than the oxide thickness $d_{ox}=500$ nm. The trap capacitance C_t is equal to $q^2D(E)$, where D is the density of trap states. To dominate the insulator capacitance, $C_t > C_{ox}$, and the charge trap density should exceed $10^{11}\ cm^{-2}\,eV^{-1}$ which is a reasonable value and is in good agreement with the temperature-dependent behavior (see below). As discussed below, we cannot be certain whether the traps are at the SiO_2/MoS_2 interface or are instead intrinsic to the MoS_2 bulk. However, it should be noted that high S values are a common problem in thin-film semiconductors.[2,3]

In the temperature range from 295 to 175 K the field-effect mobility does not change significantly, as evidenced by the nearly constant slope dI_{sd}/dV_g in Fig. 3(a). The four-probe field-effect mobility is similarly temperature independent at large negative V_g in this temperature range. The two-probe (Fig. 4) and four-probe (not shown) conductances show activated behavior, with activation energies which depend on gate voltage (Fig. 5). Two possibilities could explain this activated conductance: Schottky barriers at the elec-

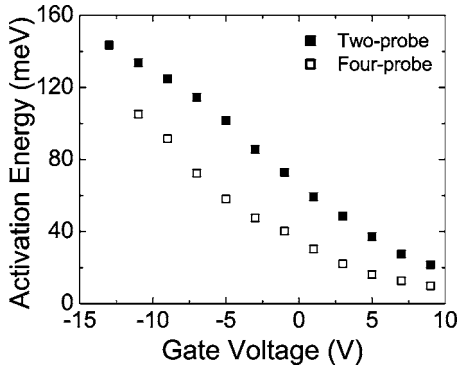

FIG. 5. Activation energy of the two-probe conductance (filled squares, extracted from Fig. 4) and four-probe conductance (open squares) as a function of gate voltage.

trodes or a large concentration of trap states. We eliminate the Schottky barrier explanation because the four-probe conductance [Fig. 3(b)] shows similar activated behavior, with a similar (though slightly lower) activation energy, also plotted in Figure 5. We then interpret the data in terms of impurity states. In Fig. 5 the two-probe and four-probe activation energies are seen to decrease roughly linearly with increasing gate voltage, with a slope of approximately $-0.006q$. We posit that the activated behavior corresponds to activation of carriers from the Fermi energy E_F to the conduction band edge or mobility edge E_c, thus the activation energy is $E_a=E_c-E_F$. This suggests that the Fermi level travels slowly through the trap states in this region; $dE_F/dV_g=-dE_a/dV_g=-0.006q$. The quantity dE_F/dV_g is given by $dE_F/dV_g=eC_{\mathrm{ox}}/(C_{\mathrm{ox}}+C_t)$. We find that $D(E)=7.2\times10^{12}$ or 9×10^{18} states/eV cm^3 for an 8-nm-thick crystal.

In order to determine whether the charge traps are bulk or interfacial in nature, we make a very rough estimate of the dopant concentration of 8×10^{17} cm^{-3} assuming a dopant density of 9×10^{18} states/eV cm^3 in a bandwidth of $\sim$90 meV (the change in E_a from $V_g=0$ to -15 V where the device appears fully depleted). This dopant concentration would correspond to a room-temperature Debye length on order 3 nm. The fact that we can fully deplete (turn off) devices of thickness 8–40 nm, much greater than the Debye length, argues that the charge traps are a surface phenomenon, not a bulk phenomenon, and that the surface density of trap states $D(E)=7.2\times10^{12}$ states/eV cm^2 is the correct measure. However, more careful measurements are needed to confirm this.

IV. CONCLUSIONS

We have successfully realized two-dimensional (2D) ultrathin transistors of MoS_2 and metallic TaS_2 films. The high on/off ratio and mobility of MoS_2 transistors can enable flexible electronics. For TaS_2, despite some evidence of disorder due to the exfoliation process, these devices show a good conductivity for a thickness in the few nanometer range and superconducting behavior at low temperature. TaS_2 nanopatches may thus be a method to realize nanometer-thickness metallic electrodes for study of other nanodevices.

ACKNOWLEDGMENTS

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